ARAB ACADEMY FOR SCIENCE, TECHNOLOGY AND MARITIME TRANSPORT

College of Engineering and Technology

Electronics & Communications Engineering Department

EFFICIENT DESIGN AND IMPLEMENTATION OF DVB-T2 MODULES ON FPGA

By

Eng. Hesham Ahmed Fahmy Amin

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Supervisors

Prof. Khaled Ali Shehata
Electronics & Communications Engineering Department
Arab Academy for Science, Technology and Maritime Transport,
Alexandria, Egypt.

Dr. Safa Mohamed Gasser
Electronics & Communications Engineering Department
Arab Academy for Science, Technology and Maritime Transport,
Cairo, Egypt.

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ABSTRACT

DVB-T2 (The second generation Digital Video Broadcasting) is a system enhancement compared to the DVB-T system. The main motivation of DVB-T2 is to provide broadcasters with more reliable, advanced and efficient alternative to DVB-T standard. The cyclic Q delay, cell interleaver and time interleaver are optional modules employed in the DVB-T2 system. The main purpose of these modules is to increase the overall performance of the DVB-T2 system. The cell mapper module is used to build the T2 frames and hence the T2 super frames. The frequency interleaver module which applies a permutation to the T2 frames is employed in the system to increase the ability of data recovery when faces the channel noise.

Combining Cyclic Q delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules into one single module is the thesis goal. The combination is to decrease the system complexity, hardware usage and the overall system delay and hence increase the overall DVB-T2 system performance. In this thesis we propose a new module to combine these modules. The new module is simulated and hardware implemented.

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LIST OF ABBREVIATIONS

64-QAM	64-ary Quadrature Amplitude Modulation
ATSC	Advanced Television Systems Committee
ACM	Adaptive Coding and Modulation
BB	Base Band
BCH	Bose-Chaudhuri-Hocquenghem error correcting code
BDCD	Bit De-interleaved and Coded Demodulation
BICM	Bit Interleaved Coding and Modulation
CI	Cell Interleaver
CRC	Cyclic Redundancy Check
DFL	Data Field Length
DTV	Digital Television
DVB	Digital Video Broadcasting
DVB-T	DVB for terrestrial broadcasting
DVB-T2	DVB-T second generation as specified in the present document
FEC	Forward Error Correction
FEF	Future Extension Frame
FFT	Fast Fourier Transform
GCS	Generic Continuous Stream
GS	Generic Stream
HDTV	High Definition Television
IFFT	Inverse Fast Fourier Transform
ISDB	Integrated Services Digital Broadcasting
LDPC	Low Density Parity Check
LSB	Least Significant Bit
MPEG	Moving Pictures Experts Group
MSB	Most Significant Bit
NM	Normal Mode
OFDM	Orthogonal Frequency Division Multiplexing
PAPR	Peak to Average Power Ratio
PLP	Physical Layer Pipe
PRBS	Pseudo Random Binary Sequence
QPSK	Quaternary Phase Shift Keying
RF	Radio Frequency
RS	Reed-Solomon
TFS	Time Frequency Slicing
TS	Transport Stream
UP	User Packet
UPL	User Packet Length
VHDL	Very High Speed Integrated Circuits

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LIST OF PUBLICATIONS

- Hesham A. Fahmy, Safa Gasser,Khaled Shehata,"Combining Cyclic Q Delay and Cell Interleaver for Enhanced Performance DVB-T2 System," *2014 The Society of Digital Information and Wireless Communications (SDIWC),* Prague Czech Republic (Published)
- Hesham A. Fahmy, Safa Gasser, Khaled Shehata " Efficient Hardware Implementation of DVB-T2 Combined Modules" *Electronics Letters* (To Be Submitted)

CHAPTER 1

INTRODUCTION

1.1 Introduction

The analog to digital video broadcasting conversion started to take place gradually with the birth of the ISDB (Integrated Services Digital Broadcasting), ATSC (Advanced Television Systems Committee) and Digital Video Broadcasting (DVB) organizations.

DVB-T which is a standard for digital terrestrial television broadcast transmission is first published in 1997 and was firstly used in Sweden and UK in1998. The DVB-T standard is the most successful digital terrestrial television standards in the world [1]. Since the publication of the DVB-T standard, however research in transmission technology has continued.

The second generation DVB standard aims to replace the current standard DVB-T or to enter the new market in the countries where analogue to digital TV is not been introduced [2], [3].

1.2 General Background

In the past few years, there has been a tremendous amount of research in the DVB-T2 area. The main motivation of digital broadcasting is to provide broadcasters with more advanced, efficient over analog in the regard of bandwidth efficiency, robustness improvement against propagation, as well as reception stability.

For the DVB-T2 system simulation, the authors in [4], [5] proposed a new error correction techniques which is a combination of both LDPC (Low density Parity Check) and BCH (Bose-Chaudhuri-Hocquengham) employed in DVB-T2. The combination technique was aimed to replace the traditional convolutional and Reed Solomon coding employed in DVB-T. In [6], [7] the authors mainly focused on researching, simulating and testing the BICM (Block Interleaving and Coding

Modulation) block in the DVB-T2 system. In their simulation and testing the authors included all possible interleaving, coding and modulation present in any BICM block carried out on a single PLP (Physical Layer Pipe). In [8] the Constellation rotation technique was analysed which is one of the features employed DVB-T2 system. The constellation rotation is known to increases system robustness. DVB-T2 standard includes two methods for PAPR (Peak to Average Power Ratio) reduction techniques which are ACE (Active Constellation Extension) and TR (Tone Reservation). The two techniques adopted for PAPR in DVB-T2 system are investigated in details in [9], [10].

For the system implementation, the implementation guidelines are illustrated in [11]. The authors in [12] designed and developed forward error correction (FEC) part for better performance DVB-T2. In [13], [14] they designed the rotated QAM Mapper/De-mapper for the DVB-T2 Standard. The authors in [15] started to design the DVB-T2 modulator modules supporting multiple PLP. In [16], [17], [18] the authors start to create new algorithms for increasing BICM performance.

1.3 Research Objective and Thesis Outline

In this research, we implement an efficient integrated hardware module that combines cyclic Q delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules for the DVB-T2 system transmitter. As a preliminary step and for verification purposes we write a Matlab program for the combined modules and then we write a VHDL code. Comparing the results of both programs is the following step. Finally synthesizing is applied using Quartus 11.2 program to check that the module is synthesizable.

Thus, this thesis is organized as follows:

Chapter 2 we give a brief overview of digital television and its related standards which are ATSC, ISDB and DVB. Afterwards the DVB system is discussed showing the basic DVB block diagram. Finally, the different standards of the DVB are mentioned briefly indicating the similarities and differences between them.

Chapter 3 we introduce the DVB-T2 system (transmitter and receiver).The system's principal features and key technologies are mentioned such as error protection, mapping, modulations, and interleaving. The algorithm of every block within the system is fully discussed.

Chapter 4 we present the Matlab simulation of the cyclic Q delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules of the DVB-T2 system in transmitter and receiver.

Chapter 5 we show the hardware implementation steps of these five modules. A VHDL program is written for every module using the FPGA Adv.Pro 8.1 program. Synthesizing is then applied showing complexity and processing time speed using Quartus 11.2.

Chapter 6 we conclude our work and also this chapter contains the future work to be done on the DVB-T2 system.

CHAPTER 2

DIGITAL VIDEO BROADCASTING

2.1 Introduction

Digital television (DTV) has become the world's very exciting topic in the television broadcasting through years. DTV along with high definition television (HDTV) services empowered by advanced digital broadcasting technologies the viewers to have the excellent watching experience with respect to the analog TV.

Thus, this chapter is divided into two sections. In section one, the different widely used digital television terrestrial broadcasting standards (DTTB) are mentioned briefly. In section two, we introduce the different DVB standards like DVB-T, DVB-T2, DVB-C and DVB-C2, focusing on the similarities and differences between them.

2.2 Digital Television Standards

2.2.1 Advanced Television System Committee (ATSC)

The Advanced Television Systems Committee (ATSC) is a standards organization created in 1982 as part of the Advanced Television Committee (ATV) [19]. The ATSC is created to promote the establishment of technical standards for all aspects of advanced television systems. ATSC has grown from 25 original organizational members to an international membership of over 200, including broadcasters, motion picture companies, telecommunications carriers, cable TV

programmers, consumer electronics manufacturers, and computer hardware and software companies.

The ATSC signals are designed to use the same 6 MHz bandwidth as analog NTSC television channels. Figure 2.1 shows the ATSC block diagram. The system consists of three main parts: Video Subsystem (or audio subsystem), Service Multiplex and Transport system and RF/Transmission System.

The Digital Television Standard is the system used to transmit high quality video and audio and ancillary data over a single 6 MHz channel. This means that encoding a video source whose resolution can be as high as five times that of conventional television (NTSC) resolution requires a bit rate reduction by a factor of 50 or higher. To achieve this reduction, the system is designed to be efficient in utilizing available channel capacity by exploiting complex video and audio compression technology. The objective is to maximize the information passed through the data channel by minimizing the amount of data required to represent it.

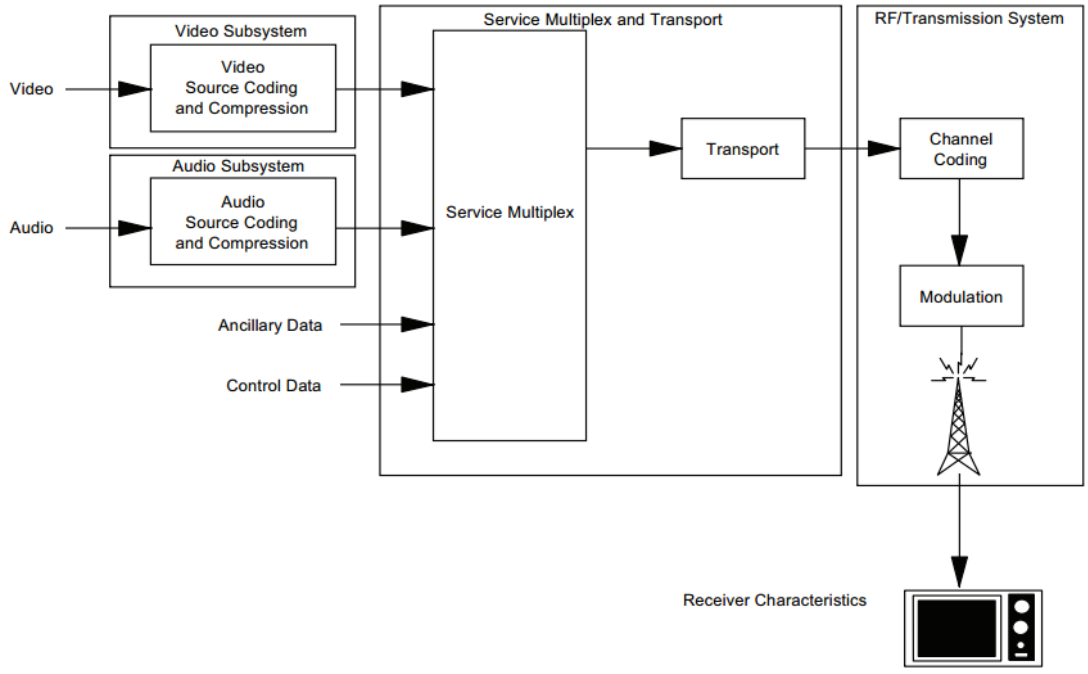

Fig. 2.1: ATSC Block Diagram [19]

The “Source coding and compression” refers to the bit rate reduction methods. The purpose of the coder is to minimize the number of bits needed to represent the audio and video information. On the other hand the “Service multiplex and transport” is a means of dividing the digital data stream into packets of information. The digital television system employs the MPEG-2 transport stream syntax for the packetization and multiplexing video, audio and data signals compression. The MPEG-2 transport stream syntax is used in applications where channel bandwidth or recording media capacity is limited. The “RF/transmission” block refers to channel coding and modulation. The channel coder takes the data bit stream and adds additional information that is used by the receiver to reconstruct the data from the received signal which, due to transmission, may not be represented accurately from the transmitted signal.

2.2.2 Integrated Services Digital Broadcasting (ISDB)

The Integrated Services Digital Broadcasting (ISDB) is a Japanese standard for digital television (DTV) and digital radio (DAB). Figure 2.2 shows the block diagram of the ISDB system.

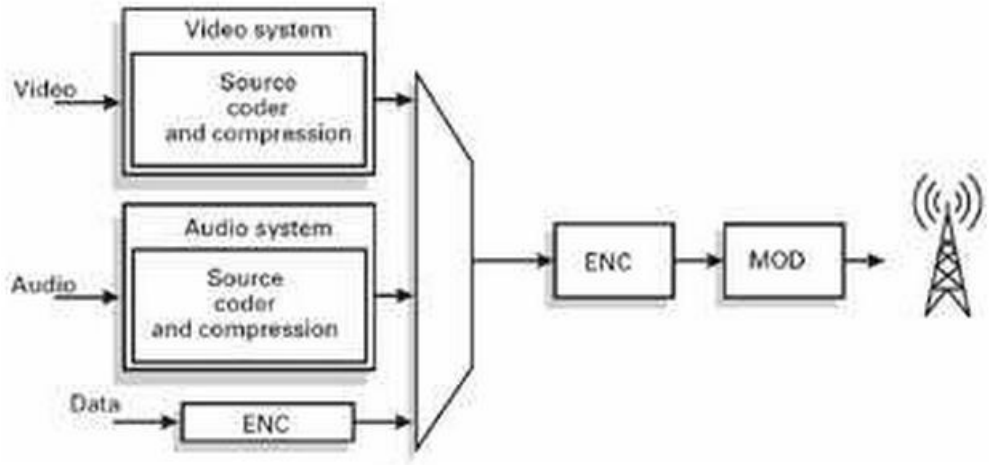

Fig 2.2 ISDB Block Diagram [20]

The ISDB is divided into three different types of systems; ISDB-C (Cable), ISDB-S (Satellite) and ISDB-T (Terrestrial) [20]. They are developed to provide expandability, flexibility and multimedia broadcasting commonality. MPEG2-TS (transport streams) can be handled by the system by employing a frame structure.

Besides audio and video transmission, ISDB also defines data connections (Data broadcasting) with the internet as a return channel over several media (10Base-T/100Base-T, Telephone line modem, Mobile phone, Wireless LAN (IEEE 802.11) etc.) and with different protocols. This is used, for example, for interactive interfaces like data broadcasting (ARIB STD-B24) and electronic program guides (EPG).

2.2.3 Digital Video Broadcasting (DVB)

The DVB project is an industry led consortium of over 270 television broadcasting associated companies world-wide. The DVB is being adopted as the standard for digital television in many countries. The committee structure of the project was committed to design an open interoperable technical standard for the global delivery of digital media and broadcast services.

The DVB system's three key standards and most commonly used standards were DVB-S for satellite networks, DVB-C for cable networks and DVB-T for terrestrial networks for data distribution. DVB then moved to embrace network convergence through the development of standards using innovative technologies that allow the delivery of DVB services over fixed and wireless telecommunications networks (e.g. DVB-H and DVB-SH for mobile TV). 2009 saw the completion of the family of second generation delivery standards; with DVB-T2 (terrestrial) and DVB-C2 (cable) joining the already published and deployed DVB-S2 (satellite). These distribution systems differ mainly in the modulation schemes used and error correcting codes used, due to the different technical constraints [21].

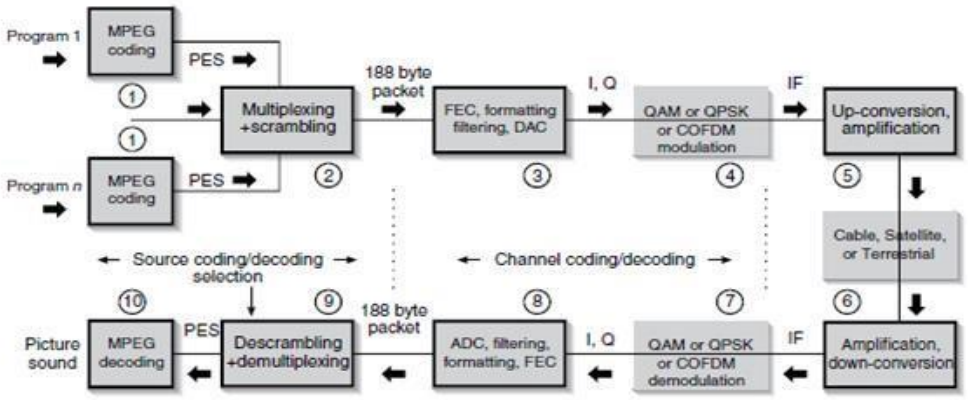

Fig. 2.3: DVB Block Diagram [21]

The basic block diagram of all DVB system is shown in figure 2.3. The system starts with a source encoder which is one of the MPEG families. The DVB-T standard uses MPEG2 while DVB-T2 uses MPEG4. The MPEG passes the video and audio packets of the programs through the multiplexer. The multiplexer uses the input packets to form 188 byte transport packets, which are eventually scrambled. After the data is packetized, it passes through a forward error correction technique (channel coding).

To increase the coding efficiency all standards use a concatenation of two encoders. The data is then mapped producing the in-phase (I) and quadrature (Q) signals. The DVB-S standard uses the QPSK scheme while the DVB-T uses the QAM (cable) or COFDM (terrestrial) and IF carrier (intermediate frequency of the order of 70 MHz).This IF carrier is then up-converted into the appropriate frequency band (depending on the medium) for transmission to the end users.

2.3 Different DVB Standards

2.3.1 Digital Video Broadcasting- Satellite (DVB- S)

The DVB-S is an abbreviation for Digital Video Broadcasting — Satellite. It was first introduced in 1993. At its core, DVB-S is a simple mechanism. Digital transmitters beam sets of channels to an area, and they are received by antennas aimed at the transmitter [22].

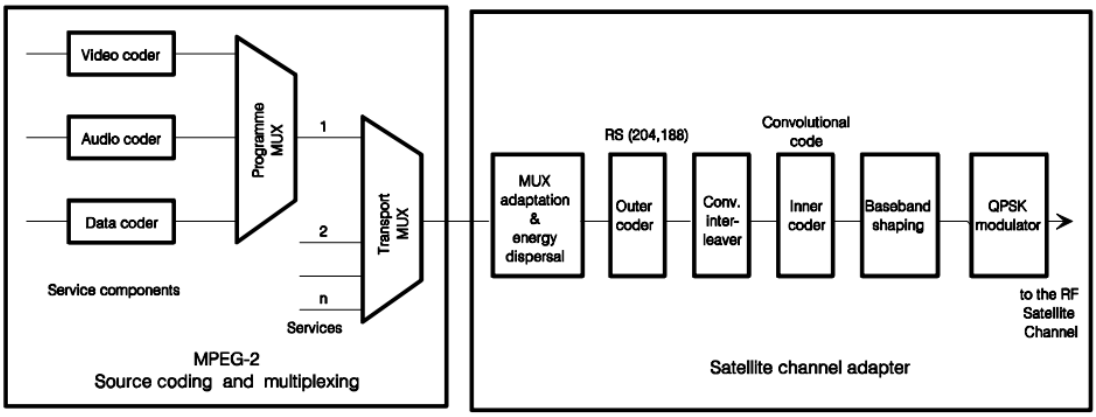

Fig.2.4: DVB-S Block Diagram [22]

The DVB-S is used in both Multiple Channel Per Carrier (MCPC) and Single channel per carrier modes for Broadcast Network feeds as well as for Direct Broadcast Satellite services.

The DVB-S system is based on QPSK modulation and convolutional forward error correction (FEC), concatenated with Reed–Solomon coding.

Figure 2.4 illustrates the block diagram of DVB-S. The System is directly compatible with MPEG-2 coded TV signals. The total packet length of the MPEG-2 transport Multiplex (MUX) packet is 188 bytes as shown in figure 2.5(a). The data of the input MPEG-2 multiplex is then randomized [22], in order to comply with ITU Radio Regulations. The data stream passes through the Reed Solomon encoder as a first step of encoding. Reed-Solomon RS shortened code, from the original RS code, is applied to each randomized transport packet (188 bytes) of figure 2.5(b) to generate an error protected packet as in figure 2.5(c).

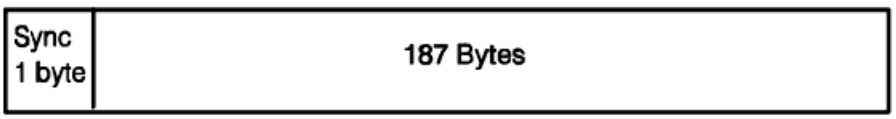

Fig. 2.5(a): MPEG-2 Transport Mux Packet [3]

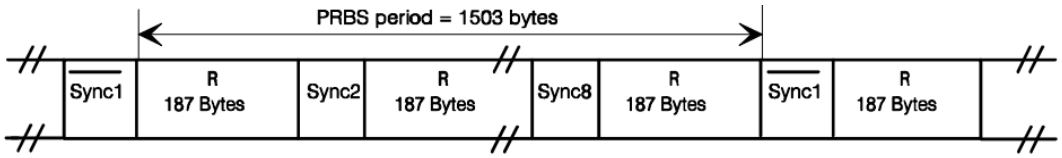

Fig. 2.5(b): Randomized Transport Packets [3]

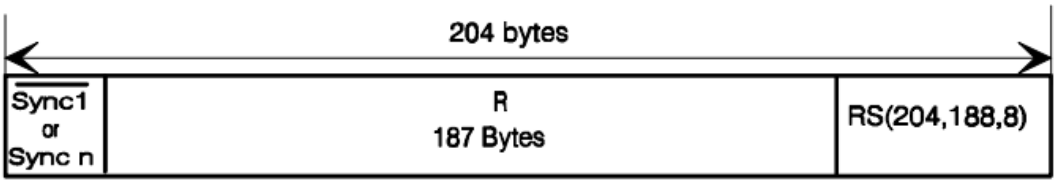

Fig. 2.5(c): (204, 188, 8) Reed Solomon error protected packets [22]

The data stream passes through the convolutional interleaving process which is based on the Forney approach. The interleaved frame is composed of overlapping error protected packets and is delimited by inverted or non-inverted MPEG-2.

After the interleaving stage the data stream passes through punctured convolutional codes. This allows selection of the most appropriate level of error correction for a given service or data rate. The System shall allow convolutional coding with code rates of 1/2, 2/3, 3/4, 5/6 and 7/8 [22].

2.3.2 Digital Video Broadcasting- Satellite Second Generation (DVB- S2)

The DVB-S2 stands for digital video broadcasting-satellite second generation. The standard is developed in 2003 by the DVB Project and ratified by ETSI in March 2005 [24]. DVB-S2 Standard represents a major step forward compared to the DVB-S one.

Figure 2.6 represents the DVB-S2 block diagram. DVB-S2 is based on a Forward Error Correction technique of BCH encoder and LDPC encoder concatenated. Furthermore, the standard encompasses a wide range of coding rates and modulation formats to achieve the best performance-complexity trade-off. DVB-S2 benefits from more recent developments in channel coding and modulation. It uses QPSK, 8PSK, 16APSK and 32APSK. The result is typically a 30 % capacity increase

over DVB-S under the same transmission conditions. This enables DVB-S2 to operate over a signal-to-noise range exceeding 18 dB exceeding by far the QPSK based DVB-S operating range which is restricted to less than 5 dB. Table 2.1 gives a comparison between both DVB-S and DVB-S2 systems.

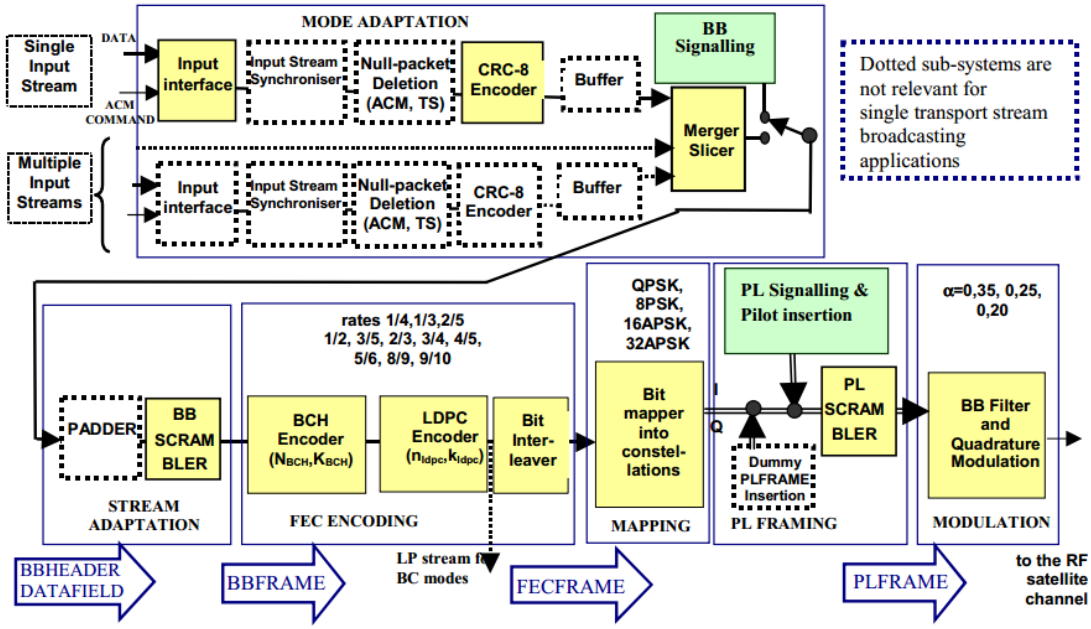

Fig.2.6: DVB-S2 Block Diagram [22]

Table 2.1: DVB-S vs. DVB-S2

	DVB-S	DVB-S2
Input Interface	Single Transport Stream (TS)	Multiple Transport Stream and Generic Stream (GSE)
Modes	Constant Coding and Modulation	Variable Coding and Modulation and Adaptive Coding and Modulation
FEC	Reed Solomon (RS) 1/2,2/3,3/4,5/6,7/8	LDPC + BCH 1/4,1/3,2/5,1/2,3/5,2/3,3/4,4/5, 5/6,8/9,9/10
Modulation	Single Carrier QPSK	Single Carrier QPSK with Multiple Streams
Modulation Schemes	BPSK,QPSK, 8PSK, 16QAM	BPSK,QPSK, 8PSK, 16APSK,32APSK
Interleaving	Bit-Interleaving	Bit-Interleaving
Pilots	Not Applicable	Pilot Symbols

2.3.3 Digital Video Broadcasting-Cable (DVB-C)

DVB-C stands for Digital Video Broadcasting-Cable. The standard was first published by the ETSI in 1994, and subsequently became the most widely used transmission system for digital cable television in Europe. Figure 2.7 shows the DVB-C block diagram. The DVB-C transmitter is similar to the DVB-S standard transmitter in most of its stages [25].

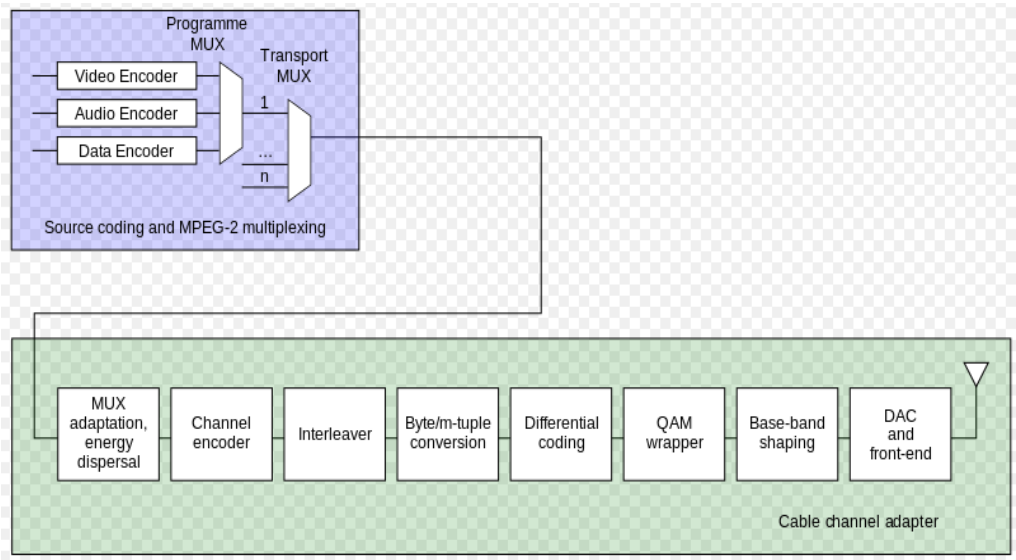

Figure 2.7: DVB-C Block Diagram [25]

The operation starts when video, audio, and data streams are multiplexed into MPEG-2 transport stream. The MPEG-TS is identified as a sequence of data packets, of fixed length (188 bytes). A first level of protection is then applied to the transmitted data, using a non-binary block code, a Reed-Solomon RS (204, 188) code, allowing the correction of up to a maximum of 8 wrong bytes for each 188-byte packet.

The data sequence passes through the external interleaver, where a convolutional interleaving is used to rearrange the transmitted data sequence, such that it becomes more rugged to long sequences of errors. After that data bytes faces the Byte/m-tuple conversion block so that the data bytes are encoded into bit m-tuples (m = 4, 5, 6, 7, or 8).

In order to get a rotation-invariant constellation, the data passes through Differential coding unit. This unit applies a differential encoding of the two Most Significant Bits of each symbol. Then the bit sequence is mapped into a base-band digital sequence of complex symbols. The system allows five modulation modes: 16-QAM, 32-QAM, 64-QAM, 128-QAM, 256-QAM. Then in order to remove mutual signal interference at the receiving side, base-band shaping block is employed, where the QAM signal is filtered with a raised-cosine shaped filter.

Finally, the digital signal is transformed into an analog signal, with a digital-to-analog converter (DAC), and then modulated to radio frequency by the RF front-end.

2.3.4 Digital Video Broadcasting-Cable Second Generation (DVB-C2)

DVB-C2 stands for Digital Video Broadcasting- Cable Second generation. The final DVB-C2 specification was approved by the DVB Steering Board in April 2009. Figure 2.8 shows the DVB-C2 transmitter. The DVB-C2 transmitter is similar to the DVB-T2 standard transmitter in most of its stages.

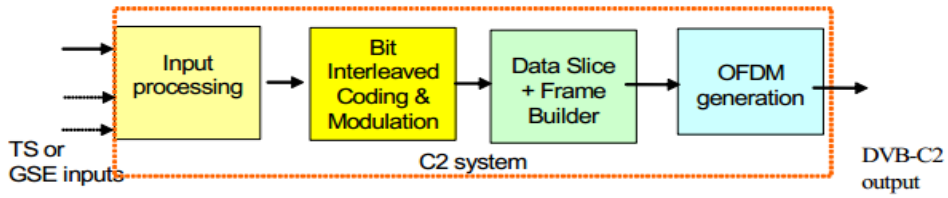

Fig. 2.8: High level C2 Block Diagram [25]

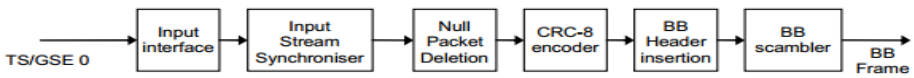

Fig. 2.9(a): Mode adaptation for single input stream (PLP) [25]

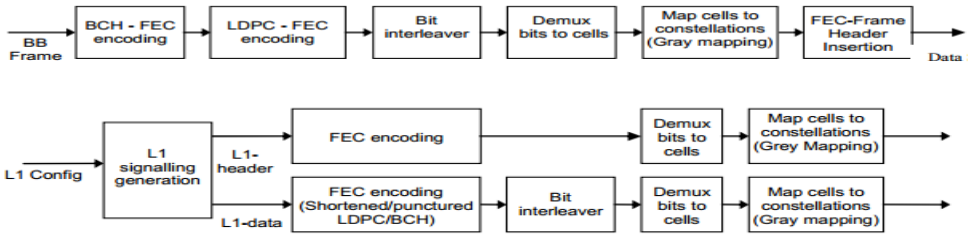

Fig. 2.9(b): Bit Interleaved Coding and Modulation (BICM) [25]

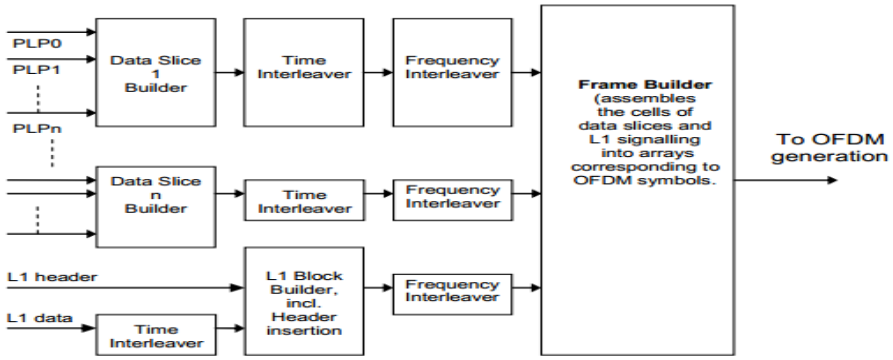

Fig. 2.9(c): Data Slice + Frame builder [25]

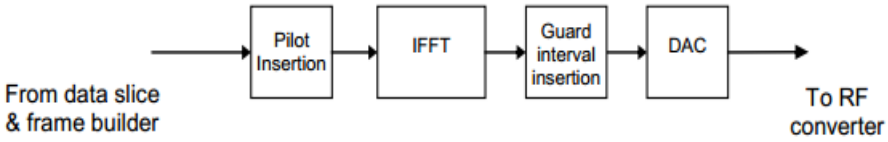

Fig. 2.9(d): OFDM Generation [25]

The input to the transmitter consists of one or more logical data streams [26]. These data streams are carried by Physical Layer Pipes (PLP). DVB-C2 uses the same Forward Error correction technique as DVB-T2 which is a concatenation of two encoders, a LDPC encoder and a BCH encoder. Then the data is interleaved, coded and modulated through the BICM stage as shown in figure 2.9(b). Each stream is de-multiplexed into N sub-streams. These N sub-streams pass through a cell mapper using a Quadrature Amplitude Modulation Scheme. The OFDM generation is the last stage which is a very simple OFDM transmitter as in figure 2.9(d) illustrates.

DVB-C2 offers greater than 30% higher spectrum efficiency under the same conditions compared to DVB-C standard, and the gains in downstream channel capacity is greater than 60% for optimized HFC networks. DVB-C2 allows bitrates up to 83.1 Mbit/s on an 8 MHz channel bandwidth when using 4096-QAM modulation;

future extensions allow up to 97 Mbit/s and 110.8 Mbit/s per channel using 64QAM and 265AQAM modulation. Table 2.2 summarizes the main differences between DVB-C and DVB-C2.

Table 2.2: The main differences between DVB-C and DVB-C2

	DVB-C	DVB-C2
Input Interface	Single Transport Stream (TS)	Multiple Transport Stream and Generic Stream (GSE)
Modes	Constant Coding and Modulation	Variable Coding and Modulation and Adaptive Coding and Modulation
FEC	Reed Solomon (RS) 1/2,2/3,3/4,5/6,7/8	LDPC + BCH 1/2, 2/3,3/4,4/5,5/6,8/9,9/10
Modulation	Single Carrier QAM	Absolute OFDM
Modulation Schemes	16- to 256- QAM	16-to 4096- QAM
Interleaving	Bit-Interleaving	Bit-Time and Frequency Interleaving
Pilots	Not Applicable	Scattered and Continual

2.3.5 Digital Video Broadcasting-Handheld (DVB-H)

DVB-H stands for Digital Video Broadcasting- Handheld. DVB-H standard is formally adopted as ETSI standard in November 2004. Figure 2.10 shows the DVB-H block diagram. DVB-H technology is a superset of the successful DVB-T system, with additional features to meet the specific requirements of handheld, battery-powered receivers.

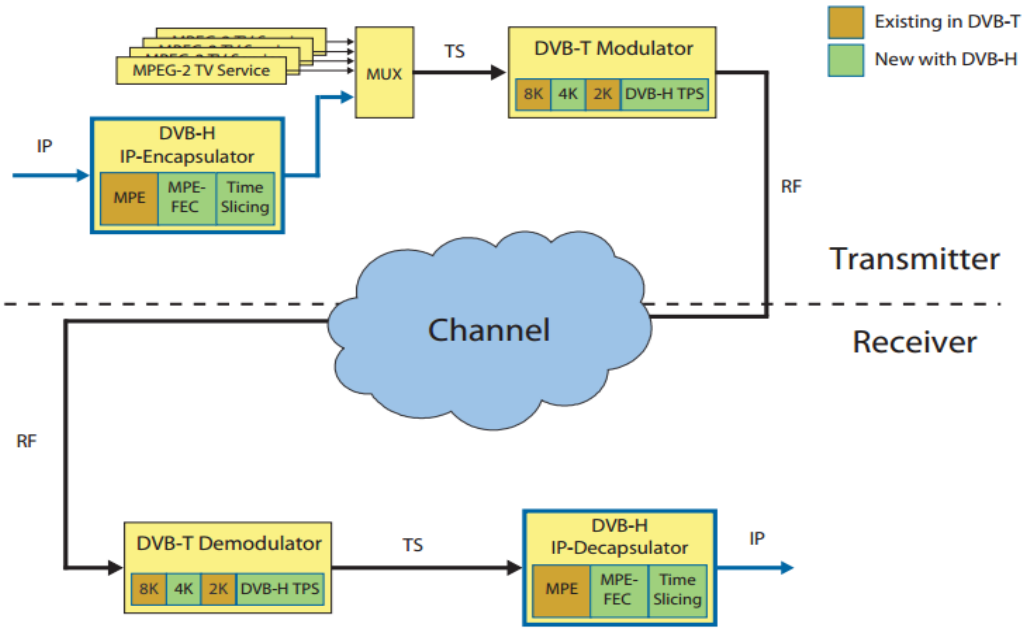

Figure 2.10: Additions brought to the DVB-T system by DVB-H [27]

DVB-H is a physical layer specification designed to enable the efficient delivery of IP-encapsulated data over terrestrial networks. DVB-H present four main requirements: broadcast services for portable and mobile usage with acceptable quality; a typical user environment, and so geographical coverage, as mobile radio; access to service while moving in a vehicle at high speed; and as much compatibility with existing (DVB-T), to allow sharing of network and transmission equipment [27].

DVB-H uses a mechanism called multi-protocol encapsulation (MPE), making it possible to transport data network protocols on top of MPEG-2 transport streams. A forward error correction (FEC) scheme is used in conjunction with this multi-protocol to improve the robustness and thus mobility of the signal. In addition to the 2k and 8k modes available in DVB-T, a 4k mode is added to DVB-H increasing the network design flexibility. A short in-depth interleaving process is introduced for 2k and 4k modes that lead to better tolerance against impulsive noise. DVB-H uses Time slicing technology to reduce power consumption for small handheld terminals.

2.3.6 Digital Video Broadcasting – Terrestrial (DVB- T)

DVB-T (Digital Video Broadcasting-Terrestrial) which is a standard for digital terrestrial television broadcast is first published in 1997. It is first used in Sweden and UK in1998. Figure 2.11 shows the DVB-T system. The main key is to transmit digital signal to offer high definition television services as efficiently and effectively as possible.

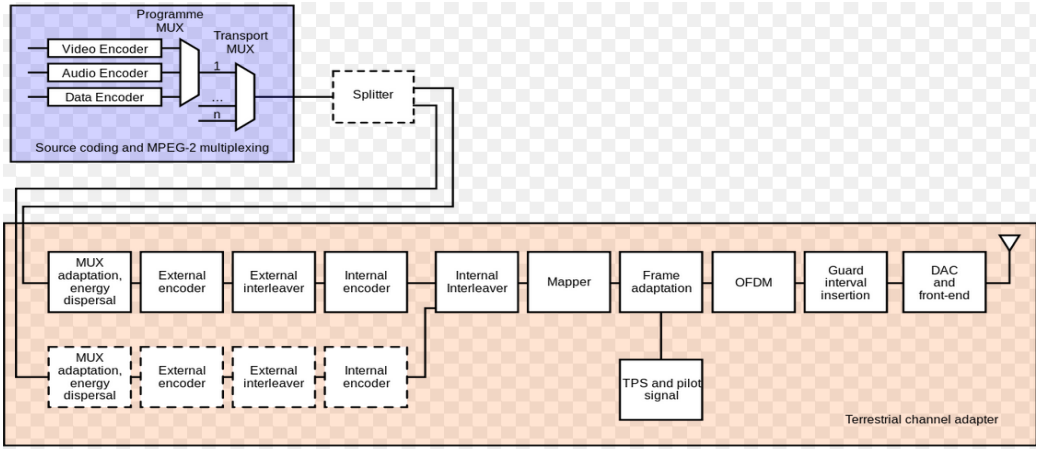

Fig. 2.11: DVB-T Block Diagram [28]

DVB-T system transmits compressed digital audio, digital video and other data in an MPEG transport stream, using coded orthogonal frequency-division multiplexing (COFDM or OFDM) modulation. There are three valid modulation schemes: QPSK, 16-QAM, 64-QAM adopted by the DVB-T [28].

The DVB-T process starts with compressed video, compressed audio, and data streams then multiplexed into an MPEG program streams (MPEG-PSs) using Source coding and MPEG-2 multiplexing (MUX) block. The resulting data stream passes through splitter where the two different MPEG-TSs are transmitted at the same time, using a technique called Hierarchical Transmission.

A first level of error correction is applied to the transmitted data, using a non-binary block code, a Reed-Solomon RS (204, 188) code, allowing the correction of up to a maximum of 8 wrong bytes for each 188-byte packet using an external encoder. The data coming out of the external encoder are then interleaved by convolutional interleaver. It is used to rearrange the transmitted data sequence.

A second level of error correction is done by the means of convolutional code used as internal encoder. The data sequence is rearranged again through an internal

interleaver, aiming to reduce the effect of burst errors. The digital bit sequence is mapped into a base band modulated sequence of complex symbols. The complex symbols are grouped into blocks of constant length (1512, 3024, or 6048 symbols per block). A frame is generated, 68 blocks long, and a superframe is built by 4 frames. Pilot signals are used during the synchronization and equalization phase. In order to simplify the reception of the signal being transmitted on the terrestrial radio channel, additional signals (Guard intervals) are inserted in each block. The sequence of blocks is modulated according to the OFDM technique (2k or 8k mode).

Finally, the digital signal is transformed into an analogue signal, by the means of a digital-to-analogue converter (DAC), and then modulated to radio frequency.

2.3.7 Digital Video Broadcasting – Terrestrial Second Generation (DVB- T2)

DVB-T2 (The second generation DVB) standard is mainly aimed to replace the current standard DVB-T. The DVB-T2 is standardized by ETSI in September 2009. The DVB-T2 is a redefined system that allows a more efficient usage substituting the extremely large DVB-T cost. The main motivation of DVB-T2 is to provide broadcasters with more advanced and efficient alternative to DVB-T standards.

The DVB-T2 system introduces a new modulation and coding techniques in comparison with DVB-T. In addition, the standard range of COFDM (Coded Orthogonal Frequency Division Multiplexing) parameters has been extended with respect to DVB-T in order to provide a greater flexibility [29].

A new error correction technique which is a combination of both LDPC (Low density Parity Check) and BCH (Bose-Chaudhuri-Hocquengham) is employed in the DVB-T2 system, aimed to replace the traditional convolutional and Reed Solomon coding employed in DVB-T.

DVB-T2 system supports different types of mapping schemes as QPSK, 16QAM, 64QAM and 256QAM. For better performance the constellations rotation and cyclic Q delay are used to uncorrelate between the in-phase and quadrature components.

DVB-T2 standard includes two new methods for PAPR (Peak to Average Power Ratio) reduction techniques, which are ACE (Active Constellation Extension) and TR (Tone Reservation) with respect to DVB-T standard. Table 2.3 gives a summary of comparison between the DVB-T and the DVB-T2 systems.

Table.2.3: The differences between DVB-T and DVB-T2

	DVB-T	**DVB-T2**
Input stream	Single stream	Multiple stream
Coding and Modulation	Constant	Variable
FEC	Convolutional coding + Reed Solomon 1/2, 2/3, 3/4, 5/6, 7/8	LDPC + BCH 1/2, 3/5, 2/3, 3/4, 4/5, 5/6
Modulation Schemes	QPSK, 16QAM, 64QAM	QPSK, 16QAM, 64QAM, 256QAM
Modulation	OFDM	OFDM
Guard Interval	1/4, 1/8, 1/16, 1/32	1/4, 19/256, 1/8, 19/128, 1/16, 1/32, 1/128
Scattered Pilots	8% of total	1%, 2%, 4%, 8% of total
Continual Pilots	2.6% of total	0.35% of total
DFT	2k, 8k	1k, 2k, 4k, 8k, 16k, 32k

2.4 Conclusion

As a conclusion this chapter covers the different digital television standards in the world like ATSC, ISDB, and DVB. In addition to each standard operation. Finally, the different DVB standards were overviewed along with the similarities and differences between them.

CHAPTER 3

DVB-T2 System

3.1 Introduction

In this chapter, we discuss the details of the DVB-T2 system specifications. Thus, this chapter is divided into two main sections. In the first section, we introduce the DVB-T2 standards. The discussion of this section is based on the DVB-T2 standard book. We discuss in details the functions of each block in the transmitter separately. In the second section, we briefly discuss the DVB-T2 receiver as it is considered the inverse of the transmitting process.

3.2 DVB-T2 transmitter

The DVB-T2 transmitter consists of four main blocks: Input processing, Bit interleaved coding and modulation (BICM), Frame builder, and OFDM generation

blocks as shown in the high level architecture of the transmitter figure 3.1. The input preprocessor which is not part of the T2 system includes a Service splitter or de-multiplexer for Transport Streams (TS) used in separating the services into the T2 system inputs. The preprocessor output is then carried in individual Physical Layer Pipes (PLPs). Figure 3.2 is the detailed DVB-T2 system architecture.

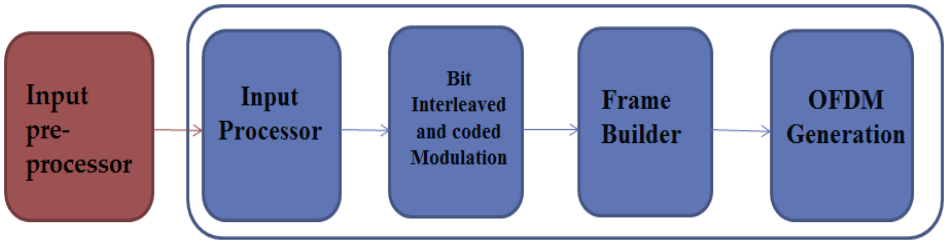

Fig.3.1: High level T2 block diagram

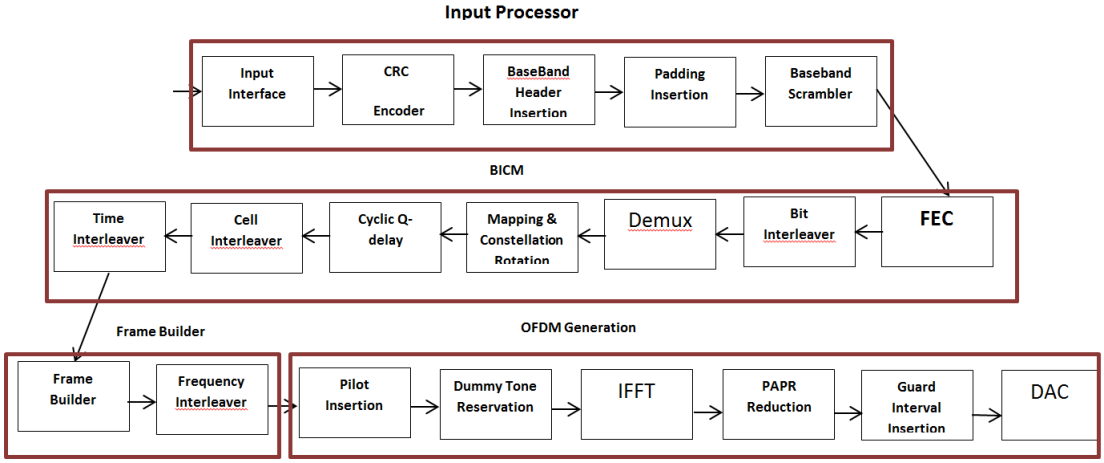

Fig. 3.2: DVB-T2 Block diagram

3.2.1 Input processor

The input processing block performs two functions as figure 3.3 shows. The first function is the mode adaptation whereas the second function is the stream adaptation.

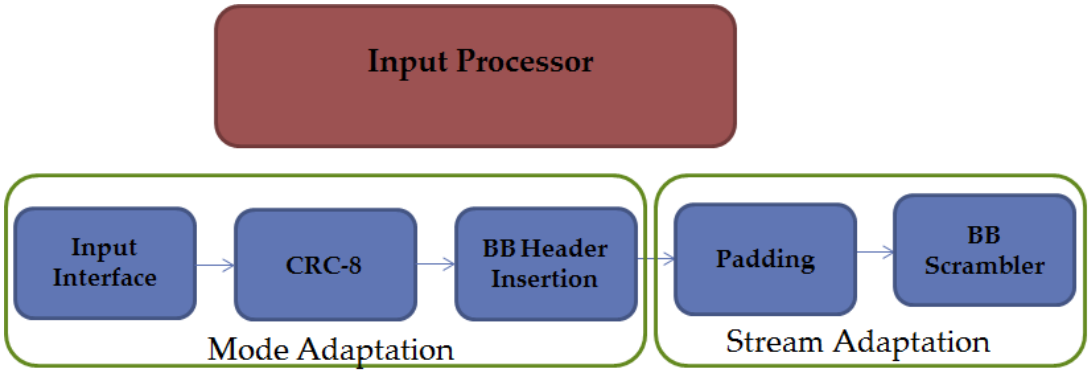

Fig.3.3: Input Processor

3.2.1.1 Mode Adaptation

The mode adaptation operates separately on the contents of each PLP. It slices the input data stream into data fields. This data field after stream adaptation will form baseband frames (BBFRAMEs).

The first block of the mode adaptation function is the Input Interface block. The input interface subsystem maps the input into internal logical-bit format. The first received bit is defined as the Most Significant Bit (MSB). The input interface reads a data field, composed of DFL bits (Data Field Length) with the condition of:

$$0 < \mathrm{DFL} < \mathrm{K_{BCH}}$$

where, K_{BCH} is the number of bits protected by the BCH encoder.

The second block of the mode adaptation module is the Cyclic Redundancy Check (CRC-8) block. It is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. Blocks of data entering the CRC encoder get a short check value attached, based on the remainder of a polynomial division of their contents; on retrieval the calculation is repeated, and corrective action can be taken against presumed data corruption if the check values do not match. The systematic cyclic codes are used to encode messages by adding a fixed-length check value, for the purpose of error detection in communication networks.

Cyclic codes are very simple to be implemented and they are well suited for the detection of burst errors. This is important because burst errors are common transmission errors in many communication channels, including magnetic and optical storage devices.

The CRC calculation is performed by means of a shift register containing n register stages, equivalent to the degree of the polynomial as figure 3.4 shows. The stages are denoted by b0 to bn. For CRC-8, the polynomial is (g0 +g1 ……+gn-1) [29].

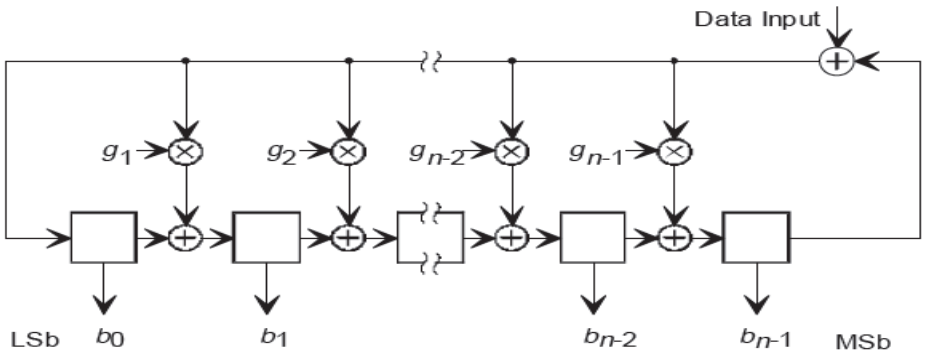

Fig. 3.4: CRC Algorithm [29]

The last block of the mode adaptation function is the Baseband header (BB-header) block. The term header refers to supplemental data placed at the beginning of a block of data being stored or transmitted. The DVB-T2 system uses a fixed length BB HEADER of 10 bytes. This header is inserted in front of the baseband data field in order to describe the format of the data field. The BB HEADER takes one of two forms: normal mode (NM) as shown in figure 3.5 (a) or high efficiency mode (HEM) as shown in figure 3.5 (b).

In the header, the input stream format and the type of Mode Adaptation is given in the MATYPE part, while the user packet length and the data field length are given in UPL and DFL parts. A copy of the User Packet Sync-byte is given in the Sync part. The distance in bits from the beginning of the DATA FIELD to the beginning of the first transmitted UP which starts in the data field is given in the SYNCD part.

The CRC-8 MODE is the XOR of the CRC-8 (1-byte) field with the MODE field (1-byte). The result of the XOR process indicates the mode used, that is if the result OD then it indicates that we have normal mode while on the other hand if the result is 1D it indicates that we have high efficiency mode [29]. ISSYI (1 bit), (Input Stream Synchronization Indicator) is active when it contains one.

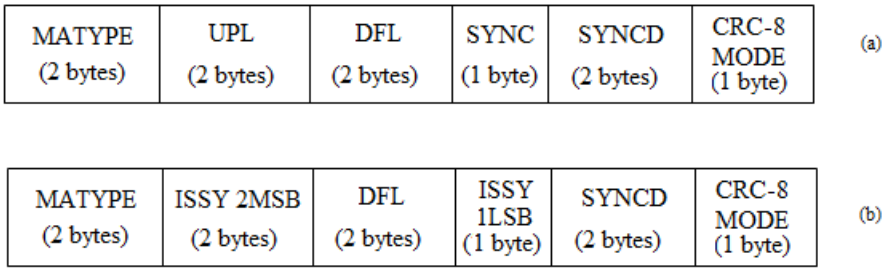

Fig. 3.5: (a) NM header format, (b) HEM header format [29]

3.2.1.2 Stream Adaptation

The first block of the stream adaptation is the Padding block. Padding is adding zeros at the beginning of the data or at the end. It is an optional feature in many communication systems. Padding does not affect the data when added. It is applied in circumstances when the user data available for transmission is not sufficient to completely fill a BBFRAME. The resulting BBFRAME after the padding operation is of a constant length of KBCH bits.

The second block of the stream adaptation is the BB scrambler block. In telecommunications, scrambler is a device that encodes or randomizes messages at the transmitter to make it unintelligible at receivers that are not equipped with appropriate descrambling device. Scrambling is widely used in satellite, radio relay communications and PSTN modems. In the DVB system the complete BBFRAME is randomized. The randomization sequence is synchronous with the BBFRAME

starting from the MSB and ending with KBCH bit. Figure 3.5 the scrambling sequence is generated by the feed-back shift register. The polynomial for the Pseudo Random Binary Sequence (PRBS) generator is:

$$1 + X^{14} + X^{15}$$

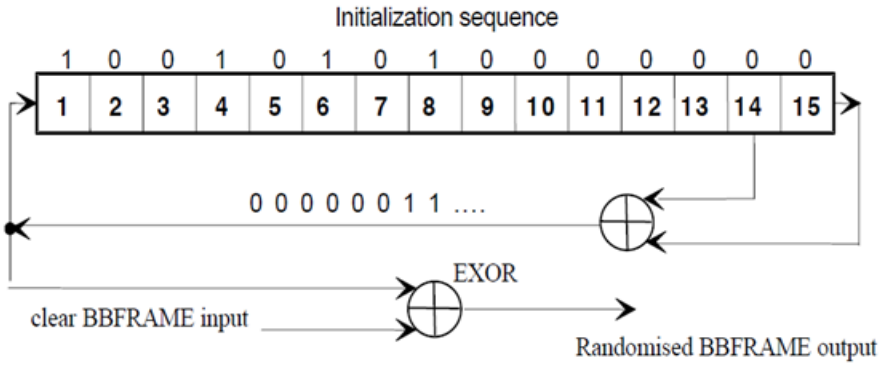

Figure 3.6: PRBS Implementation [29]

3.2.2 Bit Interleaved Coding and Modulation (BICM)

The Bit Interleaving Code Modulation is the second block of the DVB-T2 system. It consists of seven blocks as shown in figure 3.7.

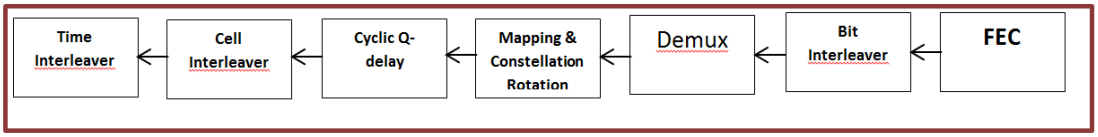

Fig. 3.7: BICM Block Diagram

3.2.2.1 FEC encoding

This sub-system shall perform outer coding (BCH), Inner Coding (LDPC) and Bit interleaving. The input stream shall be composed of BBFRAMEs and the output stream of FECFRAMEs.

Each BBFRAME (K_{bch} bits) is processed by the FEC coding subsystem, to generate a FECFRAME (N_{ldpc} bits). The parity check bits (BCHFEC) of the systematic BCH outer code is appended right after the BBFRAME, and the parity check bits (LDPCFEC) of the inner LDPC encoder shall be appended after the BCHFEC field, as figure 3.8 illustrates.

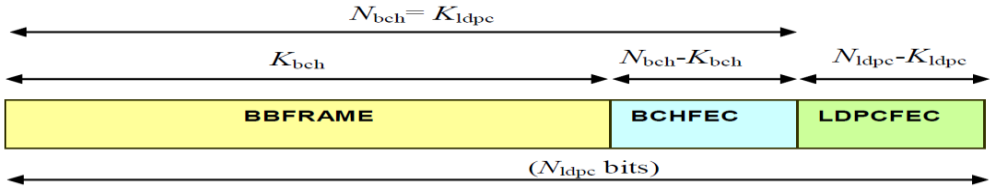

Fig. 3.8: format of data before bit interleaving [29]

- **Outer encoding (BCH)**

The outer coding BCH (Nbch, Kbch) code is the first encoding stage. It is applied to each BBFRAME for an error protected packet generation.

In coding theory, the BCH codes form a class of cyclic error-correcting codes that are constructed using finite fields. BCH codes are invented in 1959 by French mathematician Alexis Hocquenghem, and independently in 1960 by Raj Bose and D. K. Ray-Chaudhuri. The acronym BCH comprises the initials of inventors' names [29].

One of the key features of BCH codes is that during code design, there is a precise control over the number of symbol errors correctable by the code. In particular, it is possible to design binary BCH codes that can correct multiple bit errors. Another advantage of BCH codes is the ease with which they are decoded, namely, via an algebraic method known as syndrome decoding. This simplifies the design of the decoder for these codes, using small low-power electronic hardware.
BCH codes are used in applications such as satellite communications, compact disc players, DVDs, disk drives, solid-state drives and two-dimensional bar codes.

- **Inner Encoding (LDPC)**

The LDPC concept is developed by Robert G. Gallager in 1960. (LDPC) code is a linear error correcting code. It is the second encoding stage. LDPC codes are capacity-approaching codes which means that practical constructions exist that allow the noise threshold to be set very close to the theoretical maximum. The

noise threshold defines an upper bound for the channel noise, up to which the probability of lost information can be made as small as desired. Using iterative belief propagation techniques, LDPC codes can be decoded in time linear to their block length [2].

LDPC codes are finding increasing use in applications requiring reliable and highly efficient information transfer over bandwidth or return channel-constrained links in the presence of corrupting noise. Implementation of LDPC codes has lagged behind that of other codes, notably turbo codes.

3.2.2.2 Bit Interleaver

Interleaving is a technique for making forward error correction more robust with respect to burst errors. The output of the LDPC encoder is fed through a bit interleaver. The bit interleaver consists of parity interleaving followed by column twist interleaving. The bit interleaver is the second BICM stage.

In the parity interleaving part, parity bits are interleaved by [2]:

$$u_i = f_i \quad for \quad 0 \leq i < k_{ldpc} \ (information\ bits\ are\ not\ interleaved)$$

$$u_{k_{ldpc}} + 360t + s = f_{k_{ldpc}} + Q_{ldpc} * s + t, for\ 0 \leq s < 360,\ 0 \leq t < Q_{ldpc}$$

where u is the parity interleaving output and Q_{ldpc} is defined in table 3.1

Table 3.1: QLDPC values for normal frames

Code Rate	Q_{ldpc}
1/2	90
3/5	72
2/3	60
3/4	45
4/5	36
5/6	30

In the column twist interleaving part, the data bits ui from the parity interleaver are serially written into the column-twist interleaver column-wise, and serially read out row-wise (the MSB of BBHEADER is read out first) as shown in

Figure 3.9, where the write start position of each column is twisted by t_c according to table 3.2. This interleaver is described by the following [2]:

The input bit u_i with index i, for $0 \le i < N_{ldpc}$, is written to column c_i, row r_i of the interleaver, where:

$$c_i = i \operatorname{div} N_r$$
$$r_i = i + t_{c_i} \bmod N_r$$

The output bit v_j with index j, for $0 \le j < N_{ldpc}$, is read from row r_j, column c_j, where

$$r_j = j \operatorname{div} N_c$$
$$c_j = j \bmod N_c$$

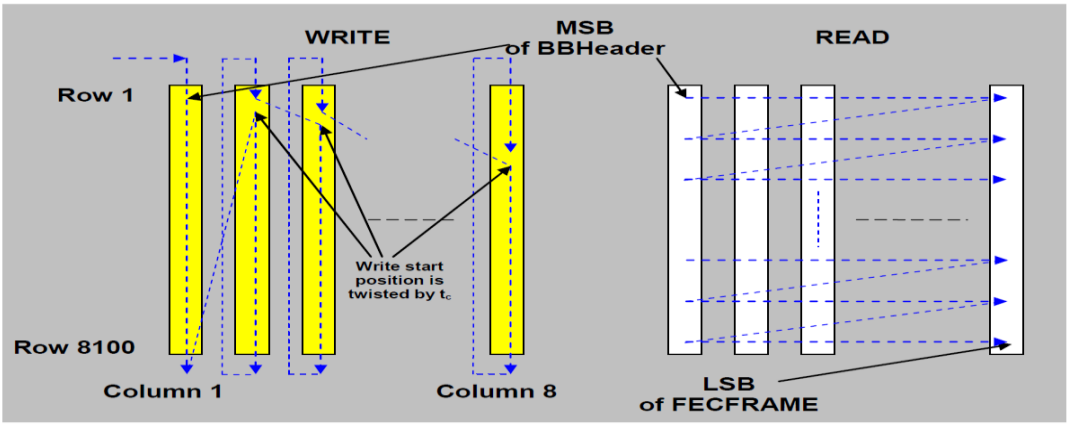

Fig.3.9: Bit interleaving scheme [29]

Table 3.2: Column twisting parameter t_c [2]

Modulation	Columns N_c	N_{ldpc}	Twisting parameter t_c															
			Col. 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16-QAM	8	64 800	0	0	2	4	4	5	7	7	-	-	-	-	-	-	-	-
		16 200	0	0	0	1	7	20	20	21	-	-	-	-	-	-	-	-
64-QAM	12	64 800	0	0	2	2	3	4	4	5	5	7	8	9	-	-	-	-
		16 200	0	0	0	2	2	2	3	3	3	6	7	7	-	-	-	-
256-QAM	16	64 800	0	2	2	2	2	3	7	15	16	20	22	22	27	27	28	32
	8	16 200	0	0	0	1	7	20	20	21	-	-	-	-	-	-	-	-

3.2.2.3 Bit to cell word de-multiplexer

The input bit-stream from the bit interleaver is de-multiplexed into N-substreams, as in figure 3.10. The number of N-substreams depends on the modulation employed as in table 3.3.

Table 3.3: Number of sub-streams in de-multiplexer [1]

Modulation	N_{ldpc}	Number of sub-streams, $N_{substreams}$
QPSK	Any	2
16-QAM	Any	8
64-QAM	Any	12
256-QAM	64 800	16
	16 200	8

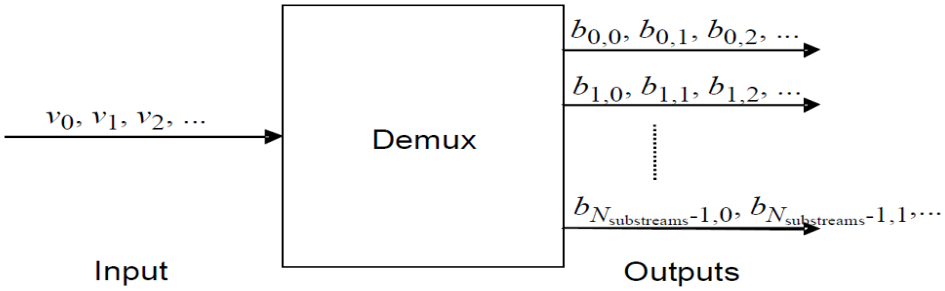

Fig. 3.10: De-multiplexing of bits into sub-streams [29]

3.2.2.4 Mapping and Constellation Rotation

The demux output for Each FECFRAME (which is a sequence of 64 800 bits for normal FECFRAME, or 16 200 bits for short FECFRAME) is then mapped into a constellation diagram as shown in figure 3.11.The input bits are grouped into cell of ηmod bits. Every modulation has a certain number of bits per cell as table 3.4 shows.

Table 3.4: Parameters for bit-mapping into constellation [29]

LDPC block length (N_{ldpc})	Modulation mode	η_{MOD}	Number of output data cells
64 800	256-QAM	8	8 100
	64-QAM	6	10 800
	16-QAM	4	16 200
	QPSK	2	32 400
16 200	256-QAM	8	2 025
	64-QAM	6	2 700
	16-QAM	4	4 050
	QPSK	2	8 100

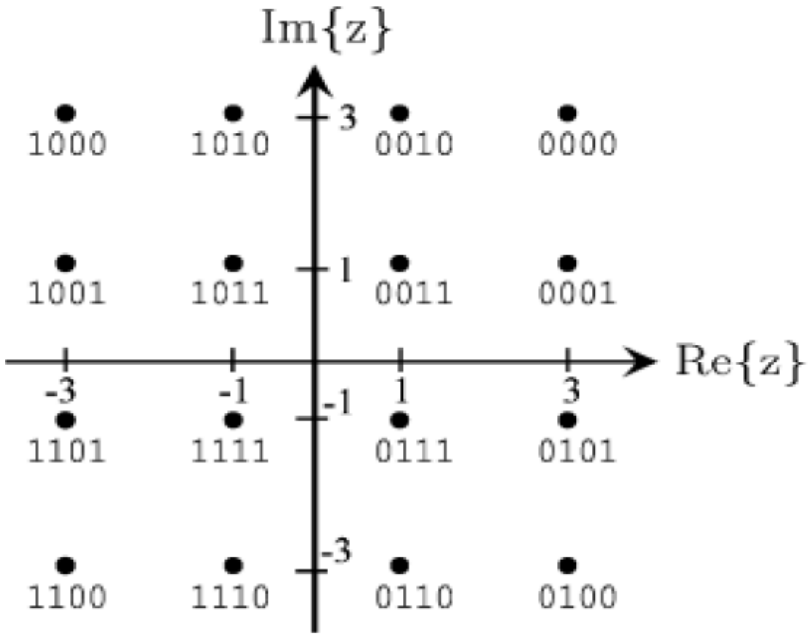

Figure 3.11: 16 QAM constellations [29]

When a constellation signal is transmitted in fading conditions, both real (I) and imaginary (Q) face the same fading. Thus, in case of severe fading, the information transmitted on I and Q channels suffer from an irreversible loss. In case of the rotated constellation, a certain rotation angle is applied in the complex plane to a classical signal constellation to uncorrelate between the two components.

The rotating of the constellation is done by the output cells G, where $G = (g_0, g_1, \ldots, g_{Ncells-1})$ are given by [1]:

$$g_0 = Re\left(R_{RQD} f_0\right) + jIm\left(R_{RQD}\, f_{N_{cells}-1}\right)$$

$$g_q = Re\left(R_{RQD} f_q\right) + jIm\left(R_{RQD}\, f_{q-1}\right)$$

where f_0 and f_q are the first and last cells respectively within the constellation diagram, RRQD is the phasor rotation angle and Φ is the rotation angle. Values of different Φ for different modulation techniques are in table 3.5. Figure 3.12 illustrates the classical constellation diagram and a rotated constellation diagram.

Table 3.5: Rotation angle for each modulation Type

Modulation	QPSK	16-QAM	64-QAM	256-QAM

Φ(in degrees)	29.0	16.8	8.6	Atan(1/16)

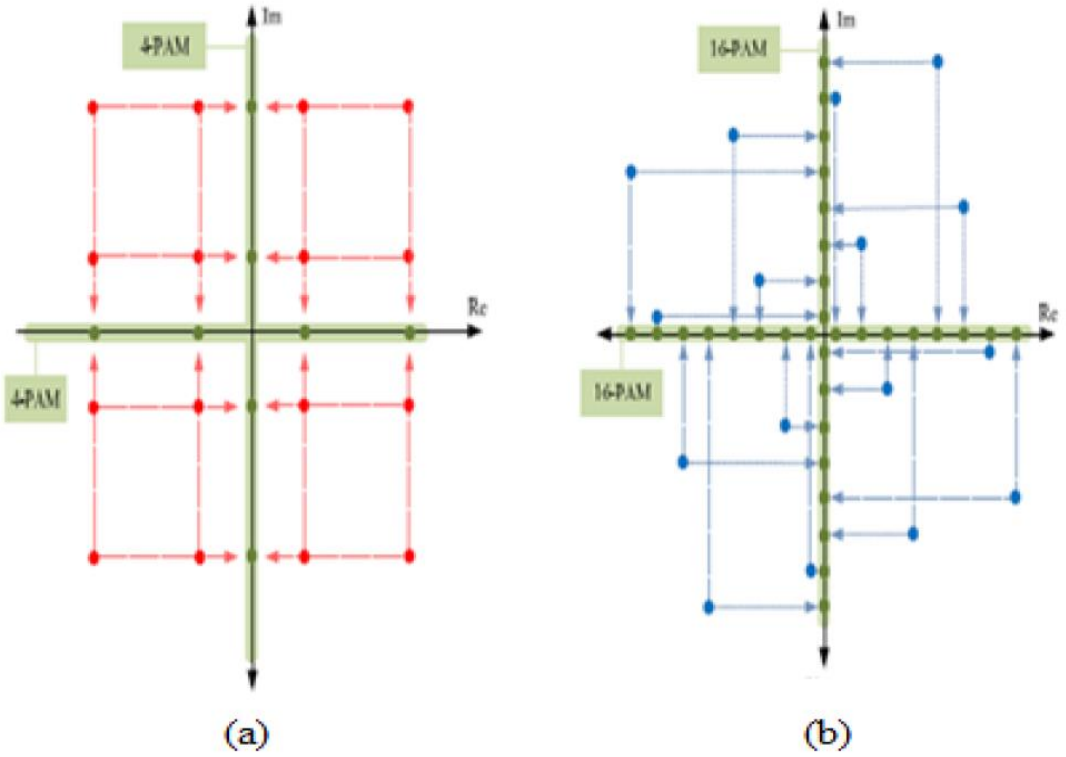

Figure 3.12: a) Classic 16-QAM constellations with projections in axis (2x 4-PAM). b) Rotated 16-QAM constellations with projections in axis (2x16-PAM) [29].

3.2.2.5 Cyclic Q-Delay

Cyclic Q delay is one of the optional modules that is used in DVB-T2. The cyclic q delay input is a stream of cells that represents the constellation rotation output. The main role of the cyclic Q delay module is to uncorrelate the real and imaginary parts (in-phase (I), quadrature (Q)) components of every constellation point especially in severe fading environment. The cyclic Q- Delay works on the

constellation rotated data $C_{in} = (C_{in1}, C_{in2}, ..., C_{in\ Ncells})$ and it delays the imaginary part by one cell. The output of the cyclic Q delay is referred to as $Co = (C_{o1}, C_{o2, ...,} C_{o\ Ncells})$, where C_o is given by:

$$Co = Re\ (C_{in\ i}) + j\ Im(C_{in\ i+1})$$

where i takes on the values 1, 2, 3 … N_{cells}. Fig.3.13 gives an illustration for the operation taking place in cyclic Q delay.

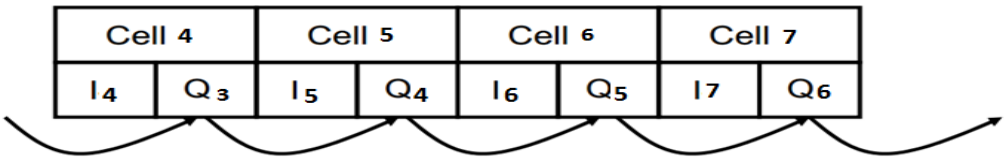

Fig.3.13: Cyclic Q-delay process [28]

3.2.2.6 Cell Interleaver

The main goal of the interleaving process is to spread the content in the time/frequency plane, such that neither impulsive noise nor frequency-selective fading would cause a long sequence of the original data stream to be erased. The cell interleaving process applies a pseudo-random permutation in order to uniformly spread the cells in the FEC code word.

The input cells to the cell interleaver take a new index generated from the pseudo random process. The Pseudo Random Cell Interleaving process that is done by the cell permutation is used to ensure an uncorrelated distribution of channel distortions in the receiver.

The input to the cell interleaver is the data cells $C_o = (C_{o\ 1}, C_{o\ 2}..., C_{o\ Ncells})$ is generated by the constellation rotation and cyclic Q delay process. The output of the cell interleaver is a vector referred to as $CI_o(j) = (CI_{o\ j,1}, CI_{o\ j,2}, CI_{o\ j,3},..., CI_{o\ j,Ncells})$. The vector is defined by: $CI_{o\ j,Sj(i)=}\ C_{o\ j,i}$,where i= 1,2,...,N_{cells} and $S_j(i)$ is the permutation function applied to FEC block j of the Time interleaver block $S_j(i) = [S_1(i) + P(j)]\ mod\ N_{cells}$, where $S_1(i)$ is the basic permutation function and P(j) is the shift value to be used in FEC block j.

For example for N_{cells}= 10800, 64 QAM, the shift P(j) is to be added to the permutation for j =1, 2, 3, etc. is 1, 8 193, 4 097, 2 049, 10 241, 6 145, 1 025, 9 217, etc. Figure 3.14 illustrates the cell interleaving process.

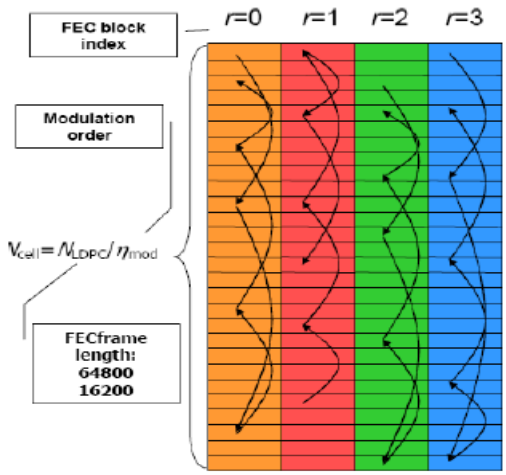

Fig. 3.14: Cell Interleaver process [29]

3.2.2.7 Time Interleaver

The cell interleaved data is introduced as an input to the time interleaver. The time interleaving process is similar to the bit interleaving process. In DVB-T2, the Forward Error Correction (FEC) blocks, for each PLP, are grouped into interleaving frames for time interleaving purposes. Each TI block contains a dynamically variable integer number of FEC blocks that are interleaved before transmission. The Time Interleaver (TI) operates at the PLP level. The parameters of the time interleaving are different for different PLPs within a DVB-T2 system. Each Interleaving Frame is either mapped directly onto one T2-frame or spread out over several T2-frames. There are three options for time interleaving for each PLP. First, each Interleaving Frame contains one TI-block and is mapped directly to one T2-frame. This gives limited data rate. Second, each Interleaving Frame is divided into several TI-blocks and each Interleaving Frame is mapped directly to one T2-frame as in Single PLP case. This gives maximum data rate. Third, each Interleaving Frame contains one TI-block and is mapped to more than one T2-frame as shown in figure 3.15.

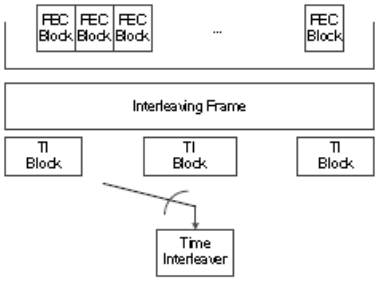

Figure 3.15: Time Interleaving Implemented in DVB-T2 [29]

The Time Interleaver is a row-column block interleaver. The number of bits of LDPC coded block Nldpc is 64 800 bits for normal FECFRAME, or 16 200 bits for short FECFRAME. The number of rows Nr in the interleaver is equal to the number of cells in the FEC block (Ncells) divided by 5 as table 3.6 shows [29].

Table 3.6: The number of rows for different modulations [29]

LDPC block length (N_{ldpc})	Modulation mode	Number of cells per LDPC block (N_{CELLS})	Number of rows N_r
64 800	256-QAM	8 100	1 620
	64-QAM	10 800	2 160
	16-QAM	16 200	3 240
	QPSK	32 400	6 480
16 200	256-QAM	2 025	405
	64-QAM	2 700	540
	16-QAM	4 050	810
	QPSK	8 100	1 620

3.2.3 Frame Builder

The frame builder block consists of 2 stages. It starts by cell mapping followed by frequency interleaving stage as shown in figure 3.16 .The cell mapper maps cells

coming from the BICM for each PLP and the signaling cells into frames of equal number of cells according to the IFFT length. The frequency interleaver then distributes the information as randomly as possible to all the DVBT2 OFDM carriers.

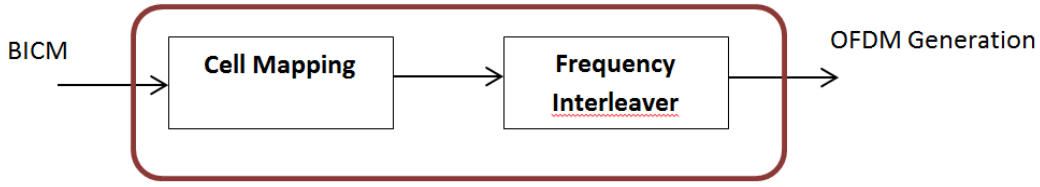

Fig. 3.16: Frame Builder

3.2.3.1 Cell Mapper

Figure 3.17 shows the Frame Structure of the cell mapper. It shows a generic T2 frame structure. At the top level, super frames define the frame structure, which are divided into T2-frames further divided into OFDM symbols.

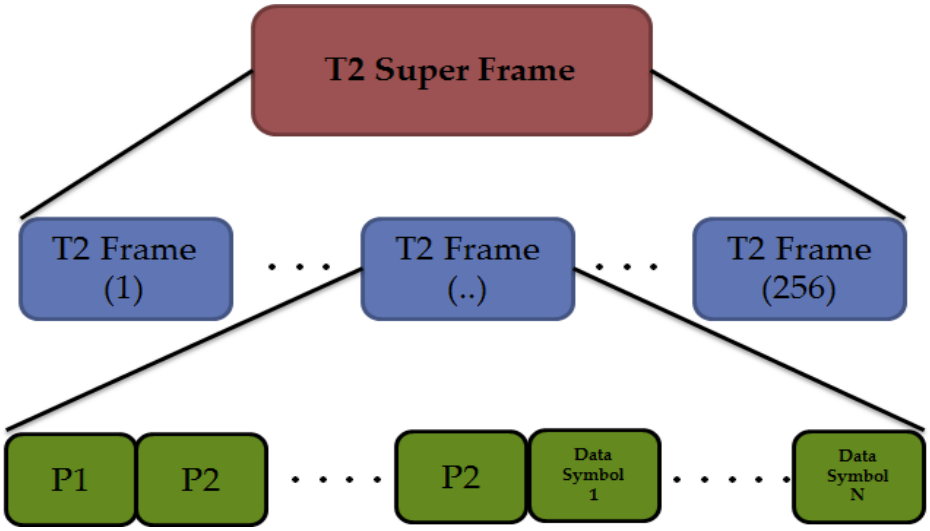

Fig. 3.17: Cell Mapper Frame Structure

The super frame contains T2-frames as well as it contains FEF (Future Extension Frames). The number of T2-frames contained in a super frame is a variable parameter configured in the L1 pre-signaling data, NT2 (NUM_T2_FRAMES). These, are marked from 0 to NT2-1. The actual frame is signaled in the dynamic L1 post-signaling. Many FEF parts can be inserted between T2- frames in a super frame. FEF parts should not be adjacent to each other. Thus the super frame duration T_{SF}:

$$T_{SF} = N_{T2} * T_F + N_{FEF} * T_{FEF}$$

where N_{FEF} is the number of FEF parts in a super frame, T_{FEF} is the duration of the FEF parts signaled by FEF_LENGTH.

In case where FEF are used, the super frame is finished by a FEF part. The maximum value for the super frame length (TSF) is 64s if FEF are not used (equivalent to 256 frames of 250ms) and 128s if FEF are used. The indexing of T2 frames and NT2 are independent of FEFs. The beginning of the first preamble symbol (P1) marks the beginning of the T2-frame. The number of P2 symbols in a T2-Frame is determined by the FFT size whereas the number of data symbols L1 data in the T2-frame is a configurable parameter signaled in the L1 pre-signaling. The maximum value for the frame duration TF is 250ms .The total number of symbols (LF) in a frame (excluding P1) is given by:

$$L_F = L_{Data} + N_{P2}$$

Thus, the maximum number for L_F is as Table 3.6 (for 8MHz bandwidth) shows.

Table 3.7 Maximum frame length LF in OFDM symbols for different FFT sizes and guard intervals (for 8 MHz bandwidth) [29]

FFT size	T_u [ms]	Guard interval						
		1/128	1/32	1/16	19/256	1/8	19/128	1/4
32K	3,584	68	66	64	64	60	60	NA
16K	1,792	138	135	131	129	123	121	111
8K	0,896	276	270	262	259	247	242	223
4K	0,448	NA	540	524	NA	495	NA	446
2K	0,224	NA	1081	1 049	NA	991	NA	892
1K	0,112	NA	NA	2 098	NA	1 982	NA	1 784

Thus the T2 frame duration is:

$$T_F = L_F * T_S + T_{P1}$$

where Ts is the total OFDM symbol duration and T_{p1} is the duration.

The frame builder maps the output cells of both the time interleaver (for the PLPs) and the constellation mapper (for theL1-pre and L1-post signaling) onto the data cells $X_{m,l,p}$ of each OFDM symbol in each frame, where: m is the T2- frame number, l is the index of the symbol within the frame.

The number of active carriers, i.e. carriers not used for pilots, in one normal symbol is denoted by C_{data}. Table 3.7 gives values of C_{data} for each FFT mode and

scattered pilot pattern for the case where tone reservation is not used. The values of C_{data} when tone reservation is used are calculated by subtracting the value in the TR

cells column from the C_{data} value without tone reservation. For 8K, 16K and 32K two values are given corresponding to normal carrier mode and extended carrier mode.

Table 3.8: Number of available data cells in one normal symbol [29]

FFT Size		Cdata (no tone reservation)								TR cells
		PP1	PP2	PP3	PP4	PP5	PP6	PP7	PP8	
1K		764	768	798	804	818				10
2K		1 522	1 532	1 596	1 602	1 632		1 646		18
4K		3 084	3 092	3 228	3 234	3 298		3 328		36
8K	Normal	6 208	6 214	6 494	6 498	6 634		6 698	6 698	72
	Extended	6 296	6 298	6 584	6 588	6 728		6 788	6 788	72
16K	Normal	12 418	12 436	12 988	13 002	13 272	13 288	13 416	13 406	144
	Extended	12 678	12 698	13 262	13 276	13 552	13 568	13 698	13 688	144
32K	Normal		24 886		26 022		26 592	26 836	26 812	288
	Extended		25 412		26 572		27 152	27 404	27 376	288
NOTE: An empty entry indicates that the corresponding combination of FFT size and pilot pattern is never used.										

3.2.3.2 Frequency interleaver

The frequency interleaver is the second stage in the frame building process. The purpose of the frequency interleaver, is to map the data cells from the frame builder onto the available data carriers in each symbol N_{data}, $N_{data} = C_{P2}$ for the P2 symbol(s). The interleaved vector $A_{m,l} = (a_{m,l,0}, a_{m,l,1}, a_{m,l,2}...a_{m,l,Ndata-1})$ is defined by: $a_{m,l,H(p)} = X_{m,l,p}$ for even symbols of the frame (l mod 2 = 0) in mode 32K for p= 0,...,N_{data}-1. $a_{m,l,\ p} = X_{m,l,H(p)}$ for odd symbols of the frame (l mod 2 = 1) in mode 32K for p = 0,...,N_{data}-1. The frequency interleaver then generates a permutation function on both the even and the odd sequence simultaneously. The permutation function employed is the same one used in cell interleaver. The frequency interleaver then combines the even and odd sequence in one output frame. The schematic block diagram of the algorithm used to generate the permutation function is as figure 3.18 presents.

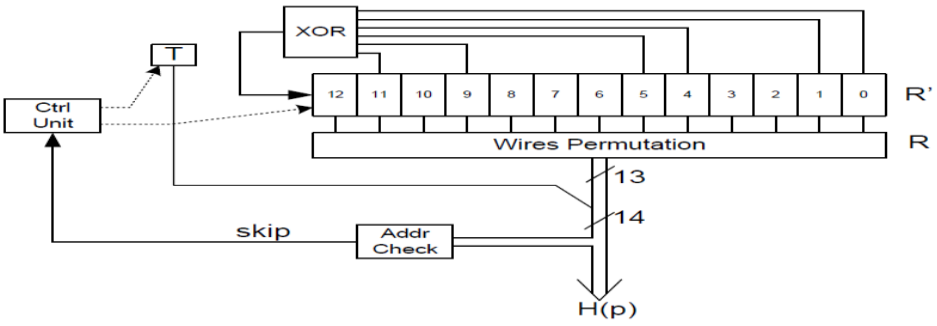

Figure 3.18: Frequency interleaver algorithm for the 16k mode [29]

3.2.4 OFDM generation

The OFDM generation is the last stage in the DVB-T2 transmitter architecture .The OFDM block consists of 6 blocks as figure 3.19 shows. The frame builder data output is fed into the OFDM generation stage. The first step is the pilot insertion which is added for channel estimation. DVB-T2 uses four kinds of pilots; Scattered, Continual, Edge, P2 and Frame Closing pilots. Data (carriers + pilots) is then fed to the IFFT process through dummy tone reservation step. Peak to average power reduction is then applied to every symbol. Finally, guard intervals are inserted to the data. Guard interval ensures that distinct transmissions do not interfere with one another. Note, The dummy tone reservation block reserves cell for PAPR.

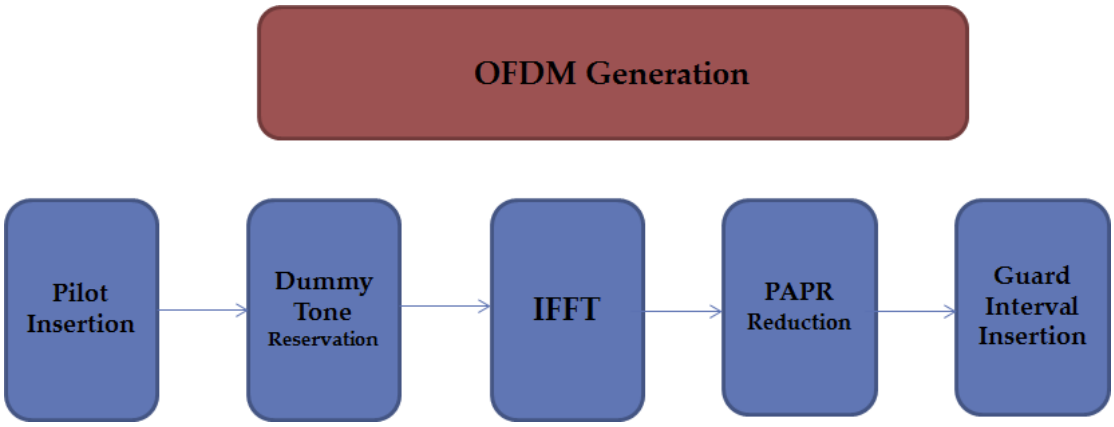

Figure 3.19: OFDM generation Block

3.2.4.1 Pilot Insertion

The pilots belong in the system as a reference information, which allow the receiver to detect and compensate for the distortions introduced by the transmission channel, and to produce from this the basis for the time domain signal for transmission. Pilots also are used for frame synchronization, frequency synchronization, time synchronization, and channel estimation. The value of the pilot information is derived from a reference sequence. The pilots are modulated according to a reference sequence, $r_{l,k}$, where l and k are the symbol and carrier indices. The reference sequence is derived from a symbol level PRBS(w_k)and a frame level PN-sequence,(PN_l). The output of the symbol level sequence, w_k, is inverted or not inverted according to the frame level sequence, PN_l, as figure 3.20 shows.

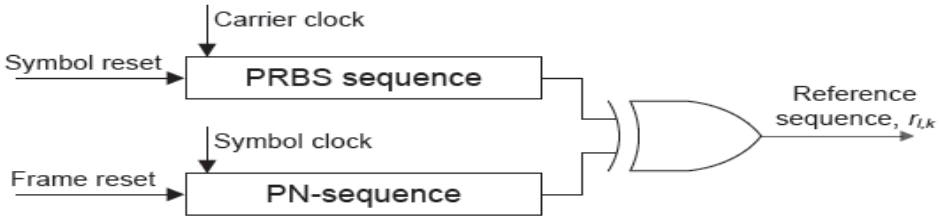

Figure 3.20: Formation of the reference sequence [29]

The symbol-level PRBS is mapped to the carriers such that the first output bit (w0) from the PRBS coincides with the first active carrier (k= Kmin) in 1K, 2K and 4K. In 8K, 16K and 32K bit w0 coincides with the first active carrier (k=Kmin) in the extended carrier mode. In the normal carrier mode, carrier k=Kmin is modulated by the output bit of the sequence whose index is Kext. This ensures that the same modulation is applied to the same physical carrier in both normal and extended carrier modes. A new value is generated by the PRBS on every used carrier (whether or not it is a pilot).

3.2.4.2 IFFT–OFDM Modulation and Guard Interval

This section specifies the OFDM structure used for transmission. The transmitted signal is organized in frames. Each frame has duration of TF, and consists of LF OFDM symbols. Each symbol is constituted by a set of Ktotal carriers transmitted with a duration TS. It is composed of two parts: a useful part with duration TU and a guard interval with duration Δ. The guard interval consists of a cyclic continuation of the useful part, TU, and is inserted before it. The allowed combinations of FFT size and guard interval are in Table 3.8.

Table 3.9: Duration of the guard interval for different FFT sizes [29]

FFT size	T_u [ms]	Guard interval						
		1/128	1/32	1/16	19/256	1/8	19/128	1/4
32K	3,584	68	66	64	64	60	60	NA
16K	1,792	138	135	131	129	123	121	111
8K	0,896	276	270	262	259	247	242	223
4K	0,448	NA	540	524	NA	495	NA	446
2K	0,224	NA	1081	1 049	NA	991	NA	892
1K	0,112	NA	NA	2 098	NA	1 982	NA	1 784

The symbols in an OFDM frame (excluding P1) are numbered from 0 to L_F–1. All symbols contain data and reference information. Since the OFDM signal comprises many separately-modulated carriers, each symbol can in turn be considered to be divided into cells, each corresponding to the modulation carried on one carrier during one symbol time. The carriers are indexed by k that belongs to K_{min} and K_{max}. The spacing between adjacent carriers is 1/TU while the spacing between carriers K_{min} and K_{max} are determined by (K_{total}–1)/TU. Some combinations of guard interval fraction and FFT size shall not be used and are marked 'NA' in the table. The emitted signal includes the insertion of guard intervals when PAPR reduction is not used. If PAPR reduction is used, the guard intervals are inserted following PAPR reduction.

3.3 DVB-T2 Receiver

In this section we introduce an overview of the DVB-T2 receiver. Figure 3.21 illustrates the block diagram of the DVB-T2 receiver. The DVB-T2 receiver consists of four main blocks as the DVB-T2 transmitter. These four blocks are the OFDM receiver block, the Frame builder block, the bit de-interleaver and decode de-modulation block and the output processor block.

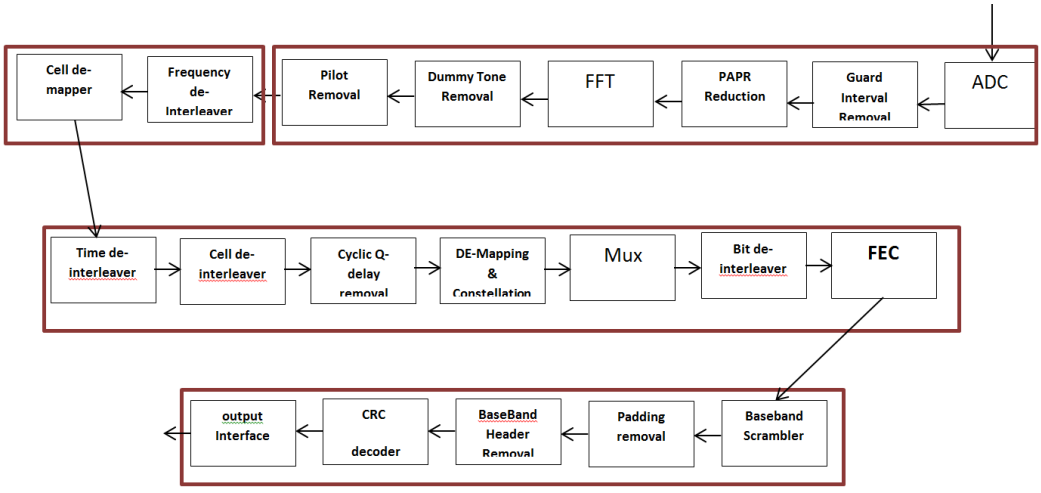

Figure 3.21: DVB-T2 system Receiver

3.3.1 OFDM Receiver Block

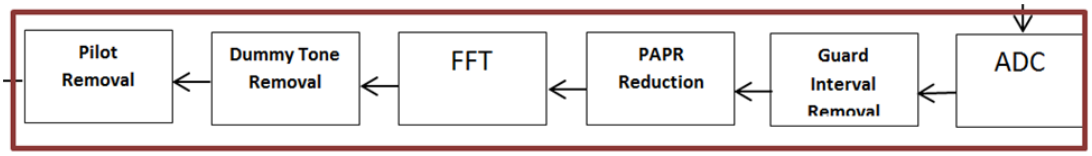

Fig 3.22: OFDM receiver block diagram

The OFDM receiver consists of 6 blocks as figure 3.22 shows, similar to that in the transmitter. The guard intervals inserted in the transmitter is removed. Guard intervals location is known to the receiver as they are between every OFDM signal. A fast Fourier transform is used to demodulate the OFDM signal. DVB-T2 is compatible with many FFT lengths like 2K, 4K, 8K……32K like that used in the IFFT process. If Peak to average power reduction is used in the transmitter dummy tone cells will be removed. Finally pilots are removed.

3.3.2 Frame Builder Block

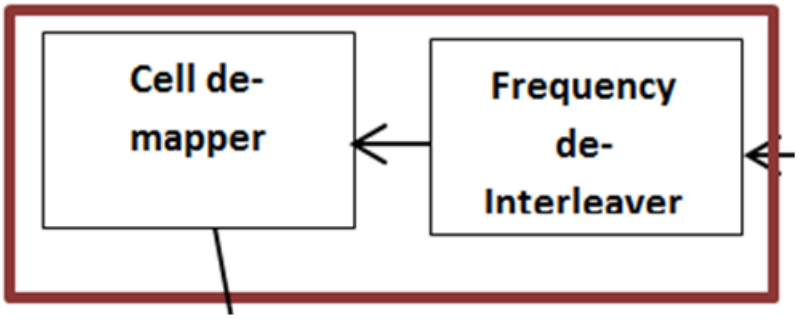

Fig 3.23: Frame builder at the receiver

Figure 3.23 shows the frame builder block which consists of two blocks. The OFDM data carriers output are deinterleaved by the frequency deinterleaver. The frequency deinterleaver is performed by two stages:

1) First, data carriers of every OFDM signal is deinterleaver, where data carriers of the even symbol is interleaved with a pattern different than that used for the data carriers of the odd symbol.

2) Second, the permutation function P(r) mentioned earlier in this chapter is performed on all data carriers. The output of the frequency deinterleaver is then fed to the cell de-mapper.

The cell de-mapper is responsible for de mapping the cells from the frequency deinterleaver that are gathered into the super frame to T2-frame which consists of a number of FEC blocks. These blocks are then deinterleaved by the time deinterleaver.

3.3.3 Bit Deinterleaved and Coded Demodulation Block

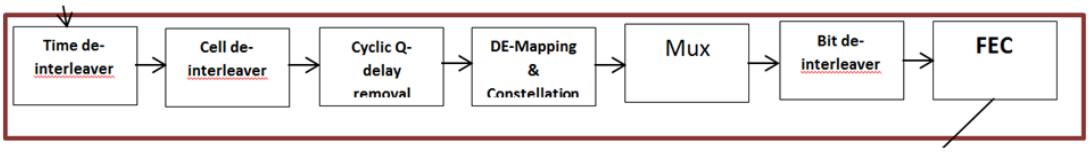

Fig 3.24: Bit De-interleaved and Coded Demodulation Block Diagram

The BDCD consists of 7 blocks as figure 3.24 shows.The Time De-Interleaver is the first step where it performs the inverse Time interleaver (TI) process. The frame builder output is fed into the time de-interleaver in the form of frames. Every frame is de-interleaved where data is written row-wise with column-wise output.

The cell de-interleaver, de-interleaves the received cells of each de-interleaved frame of the time de-interleaver. These cells are permutated using the same permutation function P(r) done on the cells used in the transmitter. Every output cell from the cell de-interleaver consists of two components the in-phase (I) and quadrature (Q). These two components are fed to the cyclic delay block. The cyclic delay removal will return the Q component shift happened on the transmitter back by one cell, such that it returned to its original position. The constellation rotation will rotate the constellation with the same angle as the transmitter returning to be a regular QAM constellation. Afterwards, every cell in the constellation will be de-mapped into bits forming the data stream ready to be multiplexed by the multiplexer. The multiplexer block first de-interleaves every cell word within each sub-stream. Then, these sub-streams are multiplexed into a single stream. The output of the stream of the multiplexer block is decoded by the BCH decoder which removes the parity bits added to the information. The output of the BCH is fed to the LDPC decoder which uses two decoding techniques knows as soft decision decoding and hard decision decoding. Finally the 80 bits of the header are removed from the received message from the LDPC decoder. Data is then descrambled and the CRC-N decoder calculates the number of errors received. Finally the original data is received at the destination.

3.4 Conclusion

As a conclusion, on this chapter we give an overview of the main funtions of the DVB-T2 system transmitter and receiver modules. We start the chapter by discussing the main block diagrams in the DVB-T2 system transmitter, where we mention the four main sub-blocks which are the input processor, BICM, the frame builder and the OFDM generation. The system's transmitter and receiver are thoroughly described.

CHAPTER 4

Matlab Simulation of the DVB-T2 system modules

4.1 Introduction

In this chapter, we give the details of the Matlab simulation of the DVB-T2 cyclic Q-delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules in transmitter and receiver. Thus, this chapter is divided into three sections. In the first section we describe the simulation details of these transmitter modules within the system. The second section we describe the simulation details of their receiver modules within the system. The third section we present the results of the simulated modules. The proposed module is built assuming 64 QAM is employed and hence the input to the proposed module is 10800 cells. The simulation is made using Matlab program version R2008.

4.2 Transmitter Simulation

The transmitter simulation is made on the cyclic Q delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules. The simulation shows the input output of these combined modules. Figure 4.1 shows the transmitter combined module. The cyclic Q delay is the first proposed module operation on the module's input stream.

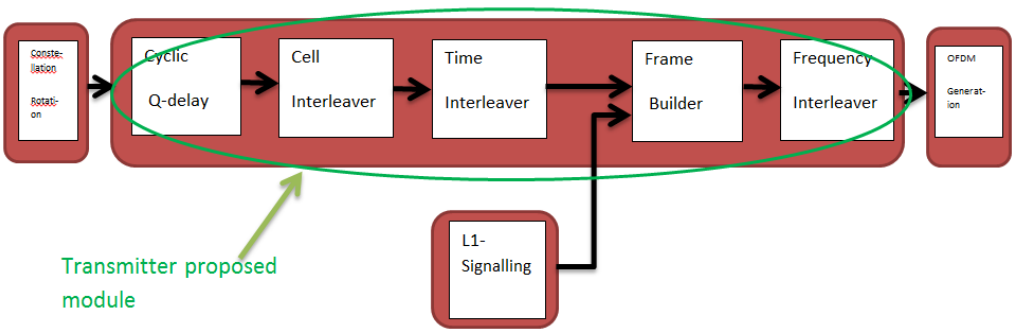

Fig.4.1: Transmitter proposed module

4.2.1 Cyclic Q-delay

The cyclic Q delay main job is to increase the overall DVB-T2 system performance by making the real and imaginary components uncorrelated to each other. The constellation rotation output which is the proposed module input is $C_{in}=(C_{in1}, C_{in2}, \ldots, C_{in\ Ncells})$. The output of the cyclic Q delay which faces the cell interleaving operation is referred to as $C_o=(C_{o1},C_{o2},\ldots,C_{oNcells})$ where Co is given by: $Co = Re(C_{in\ i}) + j\ Im(C_{in\ i+1})$

Figure 4.1 gives an illustration for the operation taking place in cyclic Q delay.

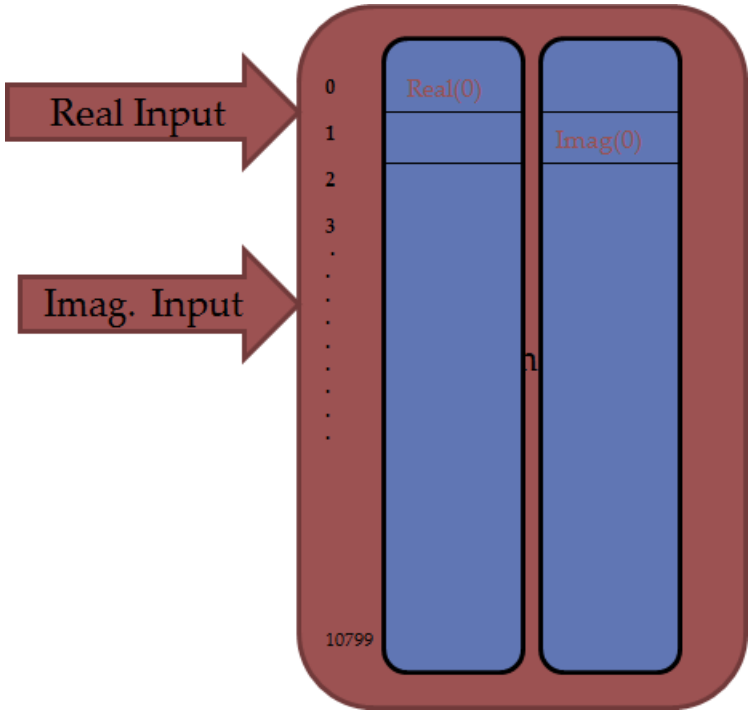

Fig.4.2: Cyclic Q-delay operation

The input to the cyclic delay block is a stream of cells of dimension (10800*1) and the output is a stream of cells of dimension (10800*1) as figure 4.3 shows. Tables 4.1 (a) and 4.1 (b) show the first and last 10 input cells respectively to the cyclic Q delay module. The first and last 10 cyclic Q delay outputs are in tables 4.1 (c) and 4.1 (d) respectively.

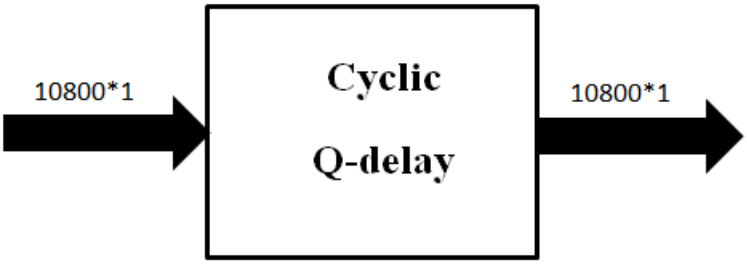

Fig.4.3: Cyclic Q-delay module input output dimensions

Table 4.1 (a): The first 10 input cells to the cyclic Q delay module

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 6.17j	5.98 + 5.8j	-7.96+ 4.49j	- 3.71 +7.36j	-1.92 -2.51j	3.41 + 2.03j	6.77 – 5j	-6.1 + 7.36j	1.92 + -0.5j	3.1+ 0.73j

Where L = 10800

Table 4.1 (b): The last 10 input cells to the cyclic Q delay module

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
7.96- 1.13j	0.83 - 4.49j	3.71 + 2.51j	-3.41 -6.4j	4.01- 3.41j	2.51 + 3.11j	0.54 - 4j	-6.4 + 4.79j	-1.73 +2j	-1.4 + 5.09j

Table 4.1 (c): The first 10 cyclic Q delay outputs

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 5.09	5.98 + 6.17j	-7.96+ 5.8j	- 3.71 +4.49j	-1.92 +7.36j	3.41 -2.51j	6.77 + 2.03j	-6.1 - 5j	1.92 + 7.36j	3.1 -0.5j

Table 4.1 (d): The last 10 cyclic Q delay outputs

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
7.96- 0.01j	0.83 - 1.13j	3.71 – 4.49j	-3.41 +2.51j	4.01- 6.4j	2.51 - 3.41j	0.54 + 3.11j	-6.4 - 4j	-1.73 +4.79j	-1.4 + 2j

Comparing between tables 4.1 (a) with 4.1 (c) and 4.1 (b) with 4.1 (d) it is clear that the Q components to the cyclic Q delay module are delayed showing that the cyclic Q delay module is working as required. The Q delayed output cells is then fed into the cell interleaver module.

4.2.2 Cell interleaver

The cell interleaving is the second process on the Q delayed output. The cell interleaving process applies a pseudo-random permutation in order to uniformly spread the cells in the FEC code word. The input cells to the cell interleaver take a new index which is generated from the pseudo random process to ensure an uncorrelated distribution of channel distortions in the receiver.

The input to the cell interleaver is the data cells C_o= (C_{o1}, C_{o2}…, $C_{oNcells}$) which is generated by the constellation rotation and cyclic Q delay process. The output of the cell interleaver is a vector referred to as CI_o (j) = ($CI_{oj,1}$, $CI_{oj,2}$, $CI_{oj,3}$,..., $CI_{oj,Ncells}$). The vector is defined by: $CI_{oj,Sj(i)=}$ $C_{oj,i}$,where i= 1,2,...,N_{cells} and S_j(i) is the permutation function applied to FEC block j of the time interleaver block $S_j(i) = [S_1(i) + P(j)] \bmod N_{cells}$ where S_1(i) is the basic permutation function and P(j) is the shift value to be used in FEC block j.

The permutation function is based on a maximum length sequence, of degree (Qn), which is given by the following equation.

Worth mentioning that, the address is discarded when it is generated with a value greater than N_{cells}. The basic permutation function S_1(i) is defined by the following algorithm:

a) For initializing the pseudo random generator of the basic permutation,

1) The toggling of the most significant bit of binary word Xi is attained by the following equation

$$\text{For } h=1: 2^{Qn}$$

$$X_h(Q_n)=h \bmod 2$$

2) Initialization of the first two is done by filling Xh(1:Qn-1) by zeros.

$$\text{For } h=1:2$$

$$X_h(1:Q_n-1)=0,0,0,\ldots,0$$

3) While the initialization of the third count is produced by filling the most significant bit by one and the rest of the bits by zeros.

For h=3

$X_h(1:Q_n-1)=1,0,0,\ldots,0$

b)1) The rest of the counts after the third is obtained by shifting the bits from 2 to Q_n-1 of the present count to take place in location 1 to Qn-2 bits in the following count. This is defined by the following equation.

For $h=4:2^{Qn}$

$X_h(1:Q_n-2)= X_h\text{-}1(2:Q_n-1)$

where Q_n-1bit is the result of Xoring different taps depending on the value of Q_n employed as illustrated in table 3.

2) For all X_h if $X_h > N_{cells}$, it is discarded from the output of the pseudo random generator.

3) For every new N_{cells} the pseudo generator adds a new value to the basic permutation Sj(i).It starts by giving a zero value to a variable k also a value of N_{cells} is given to the permutation $S_j(i)$. While $S_j(i)$ is greater than N_{cells}-1, the permutation will be as shown in the following equation:

$$P(j)=\sum_{t=1}^{Qn}[k-\lceil k/2^{t+1}\rceil/2^t]*2^{Qn-t}$$

For example using 64 QAM and hence 10800 is the number of input cells, so the shift P(j) to be added to the permutation for j = 1, 2, 3, etc. is 1, 8193, 2049, 10241, 6145, 1025, 9217, etc.

Thus the output of the cyclic Q delay is interleaved by the algorithm summarized above as figures 4.3(a-d) show.

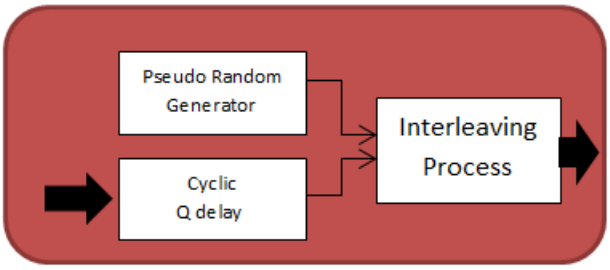

Fig.4.4 (a): Cell interleaving process

Fig.4.4 (b): Input to the cell interleaver (example)

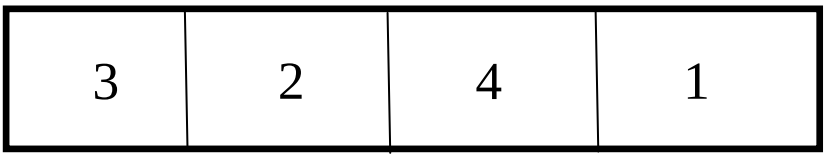

Fig.4.4 (c): Pseudo random generator output (example)

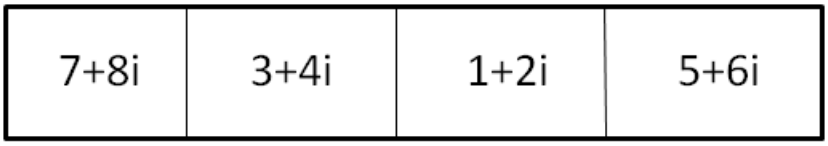

Fig.4.4 (d): The cell interleaving output (example)

The input of the cell interleaver is a stream of cells of dimension (10800*1) and the output is a stream of cells of dimension (10800*1) is as in figure 4.4. An m-file is written for the cell interleaver module. Tables 4.2 (a) and 4.2 (b) show the pseudo random permutation outputs for the first and last 10 counts respectively.

Table 4.2 (a): The first 10 pseudo random permutation output counts

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
1	8193	4097	10241	5121	10753	1281	8833	4417	10401

Table 4.2 (b): The last 10 pseudo random permutation output counts

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
963	8674	241	8313	61	8223	16	8200	4	8194

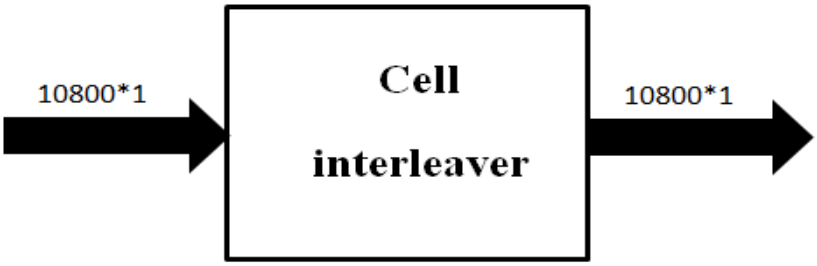

Fig.4.5: Cell interleaver input output dimensions

Tables 4.2 (c) and 4.2 (d) show the cell interleaver module outputs. The Q delayed cell interleaved cells then face the second interleaving stage by passing through the time interlaving module.

Table 4.2 (c): The first 10 cell interleaver outputs

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 5.09j	4.17 - 6.22j	-7.11 -4.8j	- 0.1 +1.89j	-5.51 -6.34j	- 1.5 + 1.08j	4.03 – 7.05j	-0.2 + 0.98j	6.28 + 1.9j	1.01+ 0.73j

Table 4.2 (d): The last 10 cell interleaver outputs

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
2.18+ 0.87j	-6.7 + 4.48j	-0.01 – 2.3j	4.27 - 7.74j	-2.7+ 6.64j	1.11 – 3.86j	5.24 - 4.91j	-4. 3 – 5.01j	-2.6 + 3j	4.07 + 6.43j

4.2.3 Time interleaver

After the first interleaving stage the stream is presented to a second interleaving stage which is the time interleaving process. The time interleaver is responsible for increasing the system immunity against long burst errors. The time interleaver input is filled column wise, while the output to the time interleaver is row wise as in figure 4.5. The time interleaver dimensions depend on the modulation scheme employed in the system, so as we designed our system using 64 QAM modulation scheme, a 2160 * 5 time interleaver is employed.

The input to the time interleaver module is a data stream of dimension (10800*1) and the output is a data stream of dimension (10800*1) as in figure 4.6.

Fig.4.6: Time interleaver input output dimensions

Figure 4.6 shows the time interleaver output operation which is the data address 0, 2160, 4320, etc.

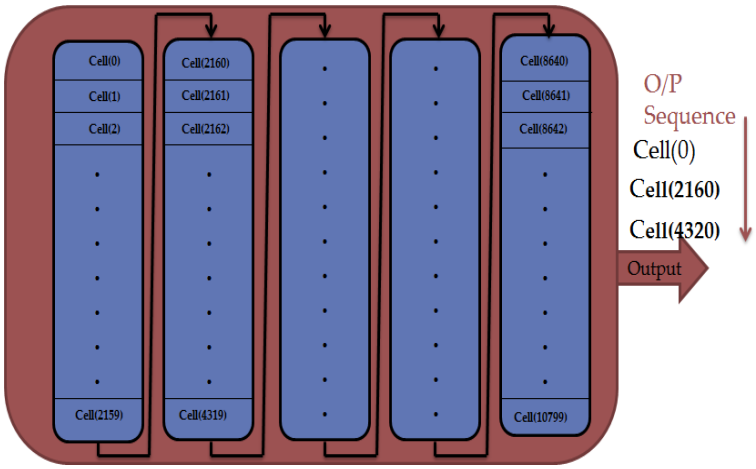

Fig.4.7: Time interleaver operation for 64 QAM

The delayed and interleaved data streams for a single PLP are then grouped with the second PLP for the frame building stage before OFDM generation stage. Tables 4.3(a) and 4.3 (b) respectively show the time interleaver output for the first PLP.

Table 4.3 (a): The first 10 time interleaver module output

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 5.09j	5.39 + 1.22j	3.01 – 4.87j	- 6.5 – 1.89l	2.51 + 6.33j	- 2.5 + 3.08j	4.02 – 2.05j	1.14 + 0.08j	5.29 – 1.74j	-4.01+ 0.37j

Table 4.3 (b): The last 10 time interleaver module output

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
-1.11+ 0.92j	5.74 + 5.38j	-0.05 – 0.1j	3.16 + 6.69j	4.7+ 0.64j	2.22 – 0.06j	-7.19 -5.9j	4.83 – 3.5j	2.08 – 4.91j	-3.9 + 1.3j

4.2.4 Frame Builder

The frame builder as figure 4.8 is used to assemble the cells produced by the time interleavers for each of the PLPs and the cells of the modulated L1 signalling data into arrays of active OFDM cells corresponding to each of the OFDM symbols which make up the overall frame structure.

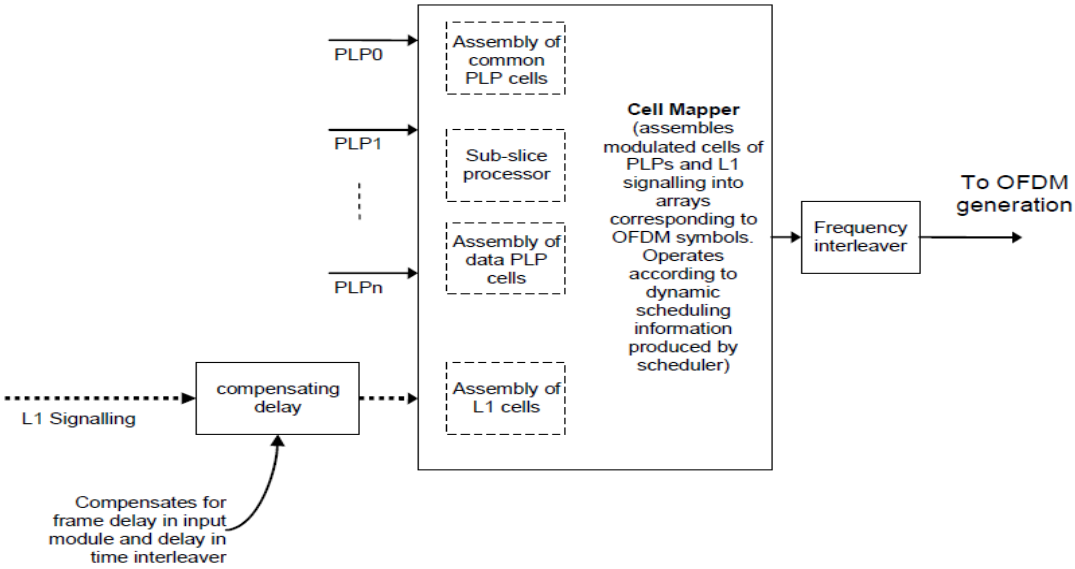

Figure 4.8: Frame builder [29]

4.2.4.1 Cell Mapper

The time interleaved data stream coming from both PLPs is introduced to the cell mapper, where it assembles modulated cells of PLPs and L1 signalling into arrays corresponding to OFDM symbols. The first and last 10 input cells to the cell mapper are as tables 4.4 (a) and 4.4 (b) show. Each time interleaver of both PLPs have a 10800 output cells and hence the cell mapper input is 10800 cells from PLPs in addition to 642 L1 signalling bits as figure 4.9 shows.

Table 4.4 (a): The first 10 cell mapper module output

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 5.09j	5.39 + 1.22j	3.01 – 4.87j	- 6.5 – 1.89l	2.51 + 6.33j	- 2.5 + 3.08j	4.02 – 2.05j	1.14 + 0.08j	5.29 – 1.74j	-4.01+ 0.37j

Table 4.3 (b): The last 10 cell mapper module output

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
-1.11+ 0.92j	5.74 + 5.38j	-0.05 – 0.1j	3.16 + 6.69j	4.7+ 0.64j	2.22 – 0.06j	-7.19 -5.9j	4.83 – 3.5j	2.08 – 4.91j	-3.9 + 1.3j

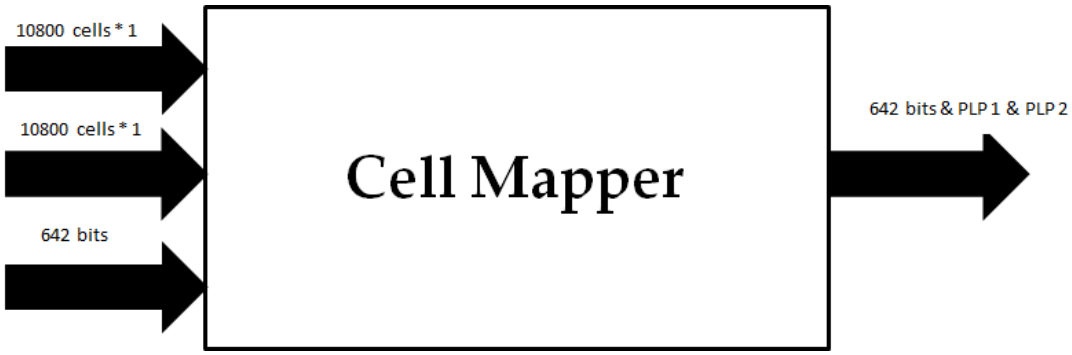

Fig. 4.9: The cell mapper input output dimensions

4.2.4.2 Frequency Interleaver

The frequency interleaver is the last interleaving stage in the DVB-T2 system. It is responsible for interleaving the data carriers of every OFDM symbol. Frequency interleaver divides the input data stream into even and odd sub-streams as figure 4.10 shows. These two sub-streams face the same permutation operation of the cell interleaver and then grouped together for transmission operation preparation done by the OFDM generation module. Figure 4.11 shows the frame builder output.

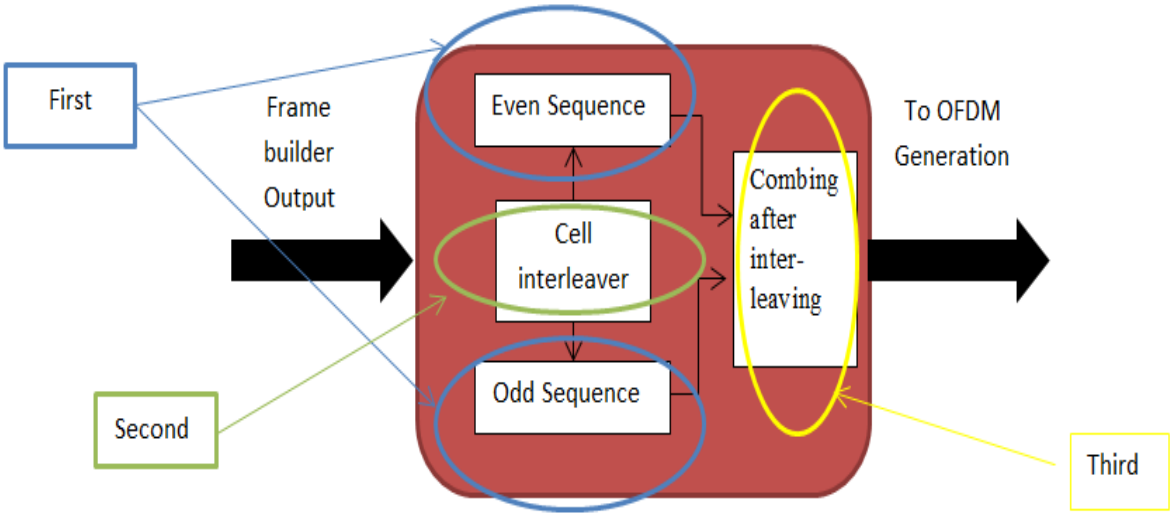

Fig.4.10: Frequency interleaver operation

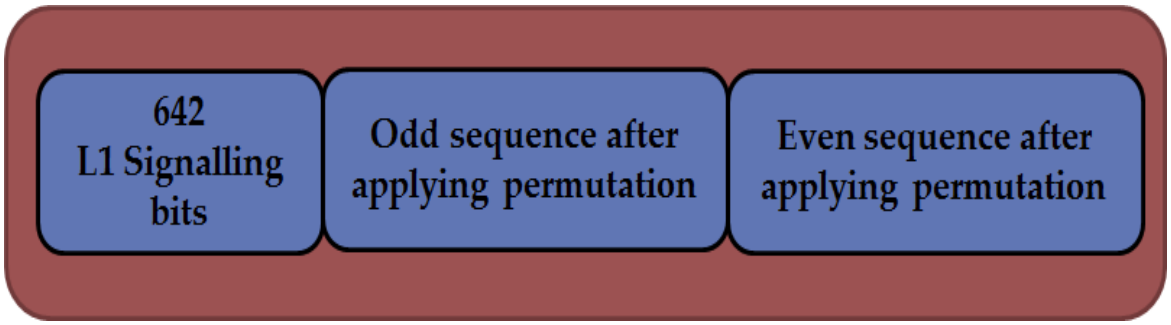

Fig 4.11: The frame builder output

4.3 Receiver Simulation

In the receiver part the inverse transmitter operation is applied on the received data stream. Figure 4.12 shows the receiver proposed module. The receiver proposed module starts by frequency de-interleaving operation followed by the cell de-mapper. The cell de-mapper output data stream is then time de-interleaved followed by the inverse permutation operation done on the transmitted data stream by the cell de-interleaver module. The cyclic Q delay removal module is the last stage in the proposed receiver module.

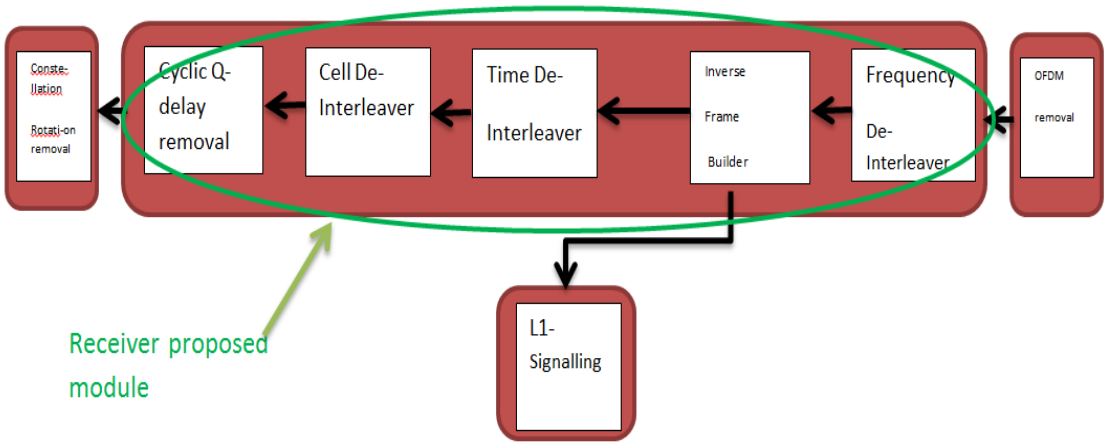

Fig.4.12: Receiver Proposed Module

4.3.1 Inverse frame builder

The inverse frame builder as figure 4.13 shows applies the reverse operation done on the transmitter. It consists of two concatenated operations. The first operation is the frequency de-interleaving operation followed by the cell de-mapping operation.

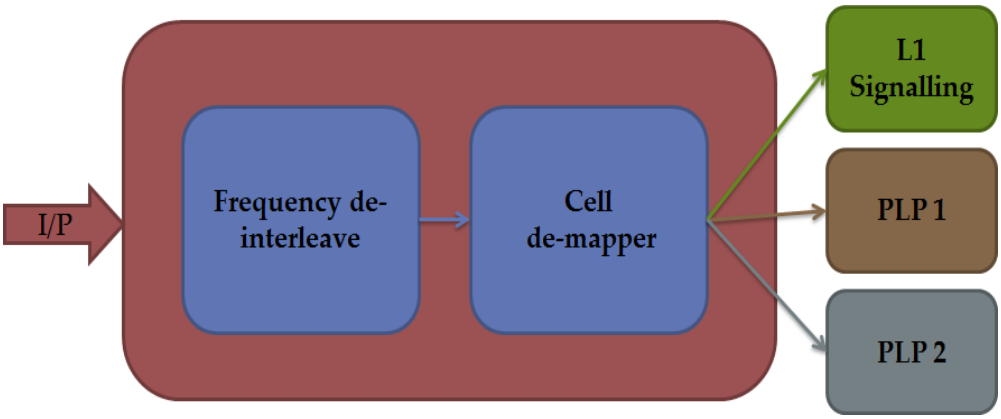

Fig. 4.13: The inverse frame builder

4.3.1.1 Frequency De-interleaver

The frequency de-interleaver is responsible for de-interleaving the received data carriers of every OFDM symbol. The input of the frequency de-interleaver is a stream of L1 signalling bits followed by 21600 cells as figure 4.14 shows. The frequency de-interleaver first divides the received data of each symbol into two 10800 cell sub-streams. The frequency interleaver then applies the inverse permutation fuction done on the data stream in the transmitter. After that it divides the sub-streams into odd and even streams before being directed into the cell de-mapper module.

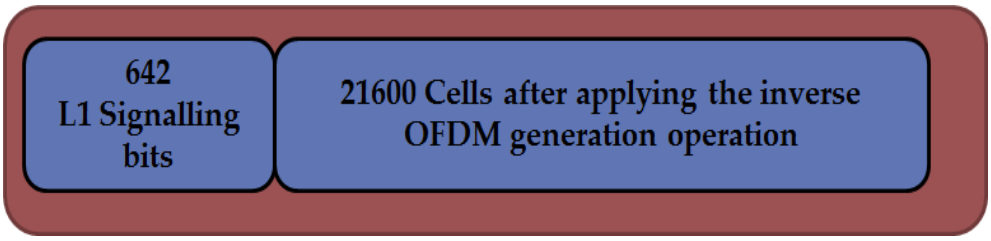

Fig 4.14: The frequency de-interleaver input data stream

4.3.1.2 Cell de-mapper

The cell de-mapper as figure 4.15 shows is used to separate the input data stream coming from the frequency de- interleaver into the original data PLPs and L1 signalling data. Its operation is the opposite one done on the transmitter side.

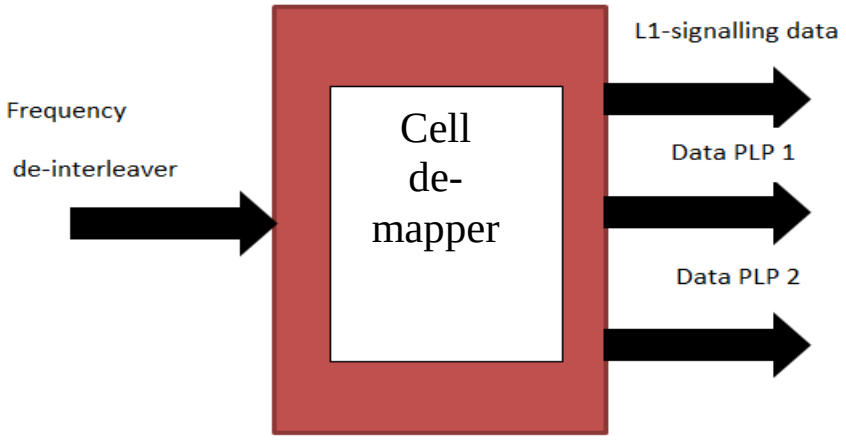

Fig.4.15: The cell de-mapper module

4.3.3 Time de-interleaver

After separating the data of both PLPs the time de-interleaver which works on PLP level has an input data stream of dimension (10800*1). The time interleaver output is a data stream of dimension (10800*1) as in figure 4.16. The time interleaver internally consists of 5 columns each column consists of 2160 rows as the same used in the transmitter side. The data input to the time interleaver is filled row wise with a column wise output. Tables 4.5 (a) and 4.5 (b) illustrate the input output data stream of the first and last 10 cells.

Fig.4.16: Time de-interleaver input output dimensions

Table 4.5 (a): The first 10 time de-interleaver outputs

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 5.09j	4.17 - 6.22j	-7.11 -4.8j	- 0.1 +1.89j	-5.51 -6.34j	- 1.5 + 1.08j	4.03 – 7.05j	-0.2 + 0.98j	6.28 + 1.9j	1.01+ 0.73j

Table 4.5 (b): The last 10 time de-interleaver outputs

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
2.18+ 0.87j	-6.7 + 4.48j	-0.01 – 2.3j	4.27 - 7.74j	-2.7+ 6.64j	1.11 – 3.86j	5.24 - 4.91j	-4. 3 – 5.01j	-2.6 + 3j	4.07 + 6.43j

Comparing the time interleaver input with the time de-interleaver output both of them having the same values ensuring that the time de-interleaver have made its role as required.

4.3.4 Cell de-interleaver

The cell deinterleaver main purpose is to recover the input data stream from the permutation done on the transmitted data stream using the same pseudo random permutation employed in the transmitter. The input is a data stream of dimension (10800*1) and the output is a data stream of dimension (10800*1) as shown in figure 4.17. The first and last 10 cell de-interleaver outputs are in tables 4.6 (a) and 4.6 (b).

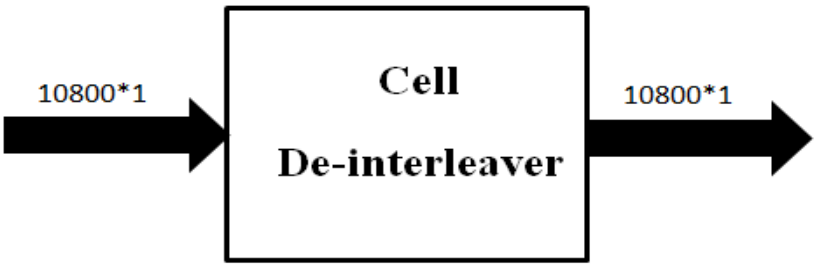

Fig.4.17: Cell de-interleaver input output dimensions

Table 4.6 (a): The first 10 cell de-interleaver outputs

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 5.09	5.98 + 6.17j	-7.96+ 5.8j	- 3.71 +4.49j	-1.92 +7.36j	3.41 -2.51j	6.77 + 2.03j	-6.1 - 5j	1.92 + 7.36j	3.1 -0.5j

Table 4.6 (b): The last 10 cell de-interleaver outputs

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
7.96- 0.01j	0.83 - 1.13j	3.71 – 4.49j	-3.41 +2.51j	4.01- 6.4j	2.51 - 3.41j	0.54 + 3.11j	-6.4 - 4j	-1.73 +4.79j	-1.4 + 2j

Comparing the cell interleaver input with the cell de-interleaver output it is found that the values of the data stream are the same and hence proving that the cell de-interleaver is working as required.

4.3.4 Cyclic Q-delay removal

The cell de-interleaver output faces the cyclic Q-delay removal which is performed only over the (Q) components. This is done in order to return the Q) components to their original position, where it was delayed by one Q component in the transmitter. The input data to the cyclic Q delay removal module is a stream of cells of dimension (10800*1) and the output is a stream of cells of dimension (10800*1) as in figure 4.18. Tables 4.7 (a) and 4.7 (b) show the cyclic Q delay removal output. Comparing tables 4.7 (a) and 4.7 (b) with the cyclic Q delay module inputs, both of them have the same value concluding that the cyclic Q delay removal is as required.

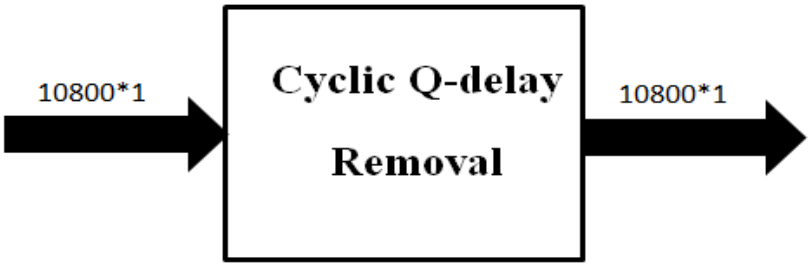

Fig.4.18: Cyclic Q-delay Removal input output dimensions

Table 4.7 (a): The first 10 input cells to the cyclic Q delay module

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24 + 6.17j	5.98 + 5.8j	-7.96+ 4.49j	- 3.71 +7.36j	-1.92 -2.51j	3.41 + 2.03j	6.77 – 5j	-6.1 + 7.36j	1.92 + -0.5j	3.1+ 0.73j

Table 4.7 (b): The last 10 input cells to the cyclic Q delay module

Cell L – 9	Cell L – 8	Cell L – 7	Cell L – 6	Cell L – 5	Cell L – 4	Cell L – 3	Cell L – 2	Cell L – 1	Cell L
7.96- 1.13j	0.83 - 4.49j	3.71 + 2.51j	-3.41 -6.4j	4.01- 3.41j	2.51 + 3.11j	0.54 - 4j	-6.4 + 4.79j	-1.73 +2j	-1.4 + 5.09j

4.4 Conclusion

In this chapter a simulation of the proposed module in the transmitter and in the receiver is made. The simulation is made on cyclic Q delay, cell interleaver, time interleaver, cell mapper and frequency interleaver modules in the transmitter side as a one module. In the receiver side simulation is made on frequency de-interleaver, cell de-mapper, time de-interleaver, cell de-interleaver and cyclic Q delay removal modules as a single module. The simulation of the proposed module is done for each module passing through the reverse module and then comparing the input of the transmitter with the receiver output. The results show that the transmitter module works as required and the receiver module has the reverse operation in recovering the data stream. The simulation is a verification step to show that these modules can be hardware implemented as a single module.

CHAPTER FIVE
Hardware Implementation

5.1 Introduction

VHDL stands for VHSIC (Very High Speed Integrated Circuits) Hardware Description Language [28]. In the mid-1980's the U.S. Department of Defense and the IEEE sponsored the development of this HDL (**H**ardware **D**escription **L**anguage) with the goal to develop very high-speed integrated circuit. It has become now one of industry's standard languages used to describe digital systems. The other widely used hardware description language is Verilog. Both are powerful languages that allow describing and simulating a complex digital systems. A third HDL language is ABEL (Advanced Boolean Equation Language) which was specifically designed for Programmable Logic Devices (PLD). ABEL is less powerful than the other two languages and is less popular in industry. Although these languages look similar as conventional programming languages, there are some important differences. A hardware description language is inherently parallel, i.e. commands, which correspond to logic gates, are executed (computed) in parallel, as soon as a new input arrives. A HDL program mimics the behavior of a physical, usually digital, system. It also allows incorporation of timing specifications (gate delays) as well as to describe a system as an interconnection of different components [30].

This chapter presents the hardware part in this dissertation. It is divided as follows: in section 5.3 the modules description of the system is presented. The QCT module which is the first system module consists of three sub-modules; Cyclic Q delay, Cell interleaver and Time interleaver where this module resembles the function of these combined sub-modules. The second module which is the frame builder consists of two sub-modules; the cell mapper and frequency interleaver. The second section presents the integrations of these five modules cyclic Q delay, cell interleaver, time interleaver, frame builder and frequency interleaver into only two modules. The third section presents the design synthesis and mapping.

5.2 DESIGN AND IMPLEMENTATION STEPS

The design and implementations steps are in figure 5.1. The first implementation step is the design entity step. The design entry tools are tools use a high-level language to describe the detailed function and actions by the designed blocks in response to different inputs. Five techniques are implemented, which are the cyclic Q-delay, cell interleaver, time interleaver, cell mapper and frequency interleaver techniques. The five techniques were implemented in only two concatenated modules.

The verification and simulation of the VHDL code representing the design is an essential step. The role behind these steps and the tool used to perform them is to verify the design's operation before a prototype is built. Simulators reduce development time by stating the errors in an early stage in the design cycle. FPGA Advantage Pro8.1 ModelSim simulation tool is used to simulate the design.

The functional simulation is done after writing the VHDL code of the designed module. It is used to test the functionality of the design in which external inputs are applied to the module and the design outputs are observed. The inputs are given in a form of a test bench of force by the user running the ModelSim software. The outputs are obtained in the form of a waveform. The functional simulation is done to whole system.

Adding design constraints comes as the design next level. Synthesizing comes after that showing if the design is synthesizable or not using Quartus II which is used in our designing steps. The synthesizing step also shows the design performance and design size.

Placing and routing the design comes after checking the design size and performance. The downloading to the device is in the end of the design implementation steps.

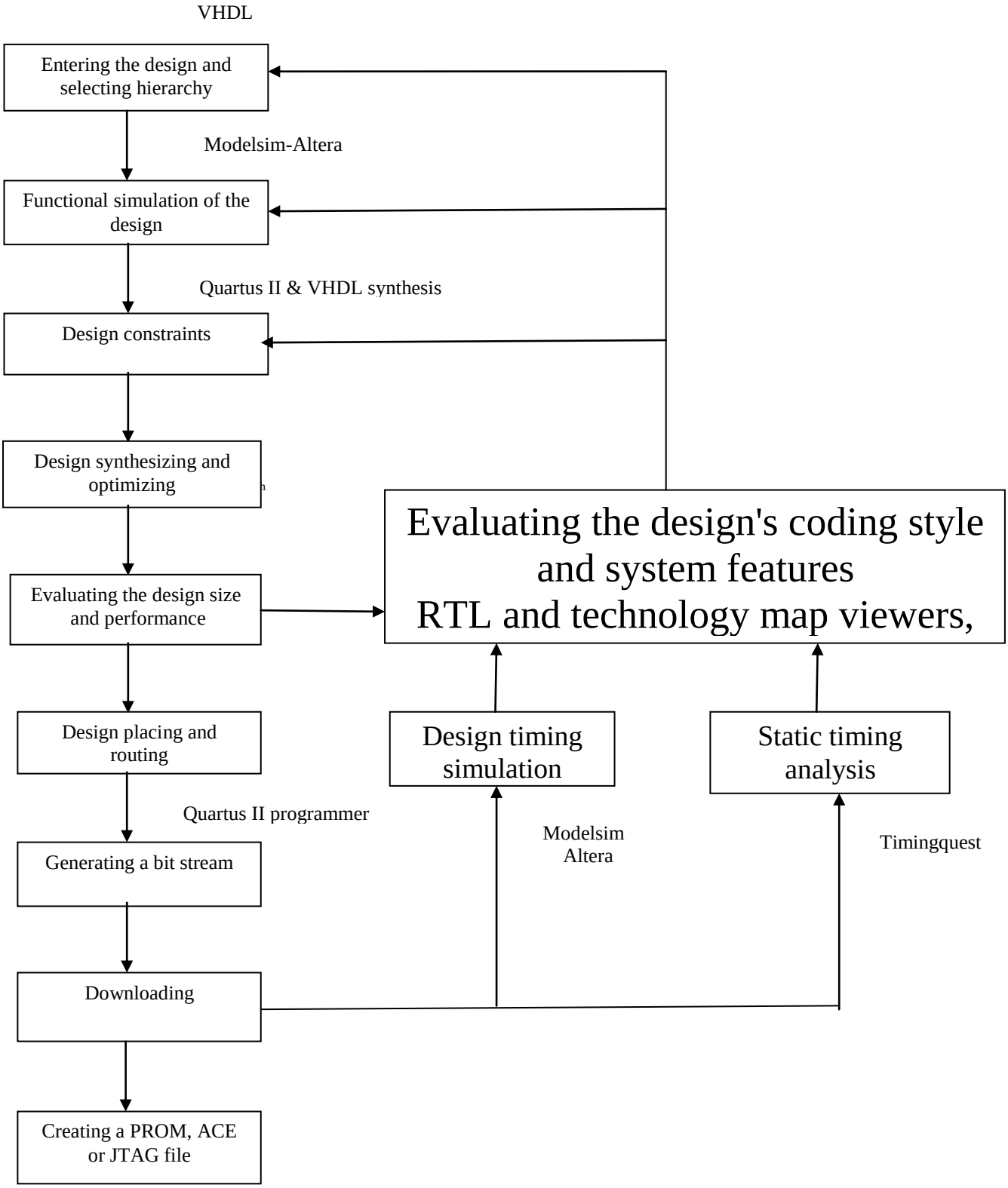

Fig. 5.1: Design and implementation steps

Fig. 5.1: Design and implementation steps [9]

5.3 Implementation of the QCTCF Module

The system main goal is to reduce the hardware area of the DVB-T2 system and hence reducing the overall cost as well as the overall system delay. The QCTCF module as in fig. 5.2 consists of two modules the QCT (Q delay, Cell interleaver and Time interleaver) module and CF (Cell mapper and frequency interleaver) module as in fig. 5.3. The QCT module is the first stage. The QCT module consists of three sub-modules the cyclic Q delay, the cell interleaver and the time interleaver. It makes the function of these three modules, in the same time decreases the overall system delay. The input data stream to the QCT module format as figure 5.4 shows. The data stream then faces the second stage which is the frame builder module. The frame builder module makes the role of both the cell mapper and the frequency interleaver.

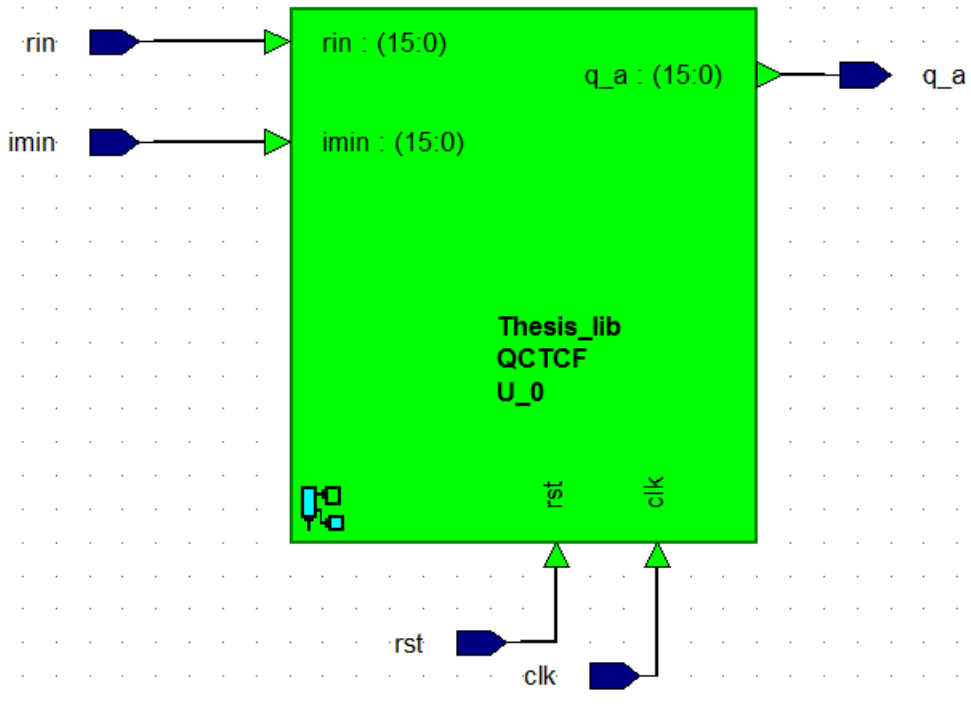

Figure 5.2: QCTCF Module

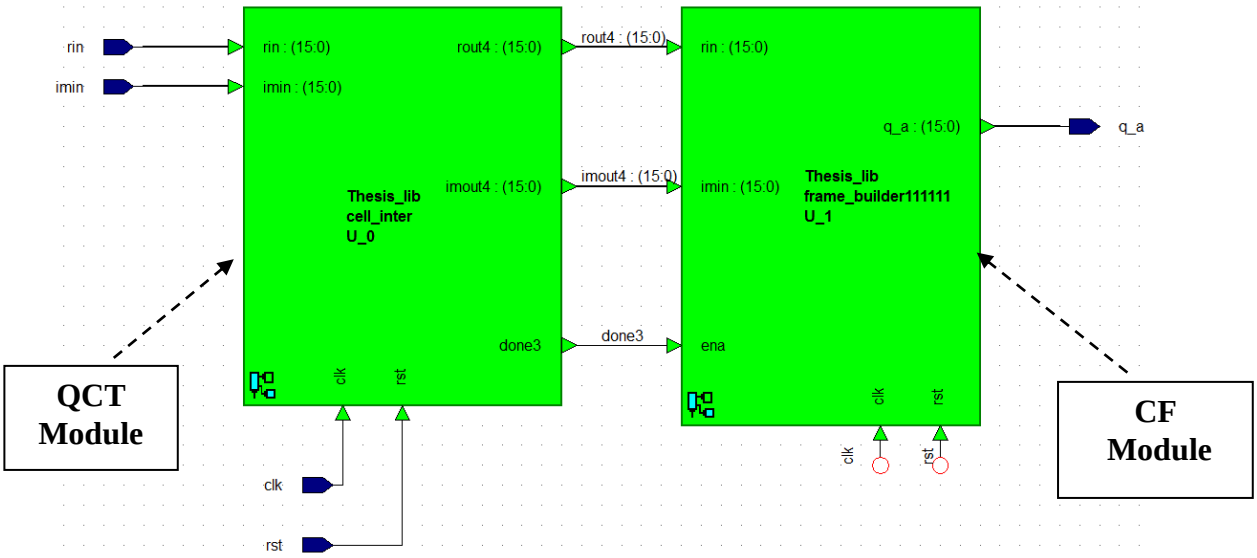

Figure 5.3: QCT and CF Module

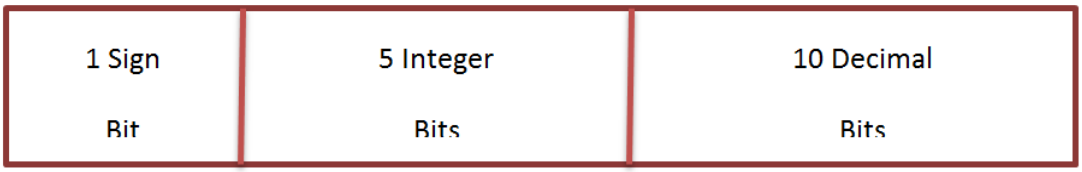

Figure 5.4: The data input format for each clock for I and Q components

5.3.1 The QCT Module

The QCT module stands for Q delay, Cell interleaver and Time interleaver. It is the first module which makes three different operations within the DVB-T2 system. The QCT module applies cyclic Q delay, cell interleaving and time interleaving operations on the input data stream. Both cyclic Q delay and cell interleaver operations are applied to the input data stream with time interleaving operation QCT output. The QCT module depends on a RAM of 10800 * 2 size. The QCT module has four input ports with three output ports. The first two ports are the I and Q components data stream (r_{in} and im_{in}). The other two ports are the reset and the system clock. The QCT module output then passes through the frame builder module.

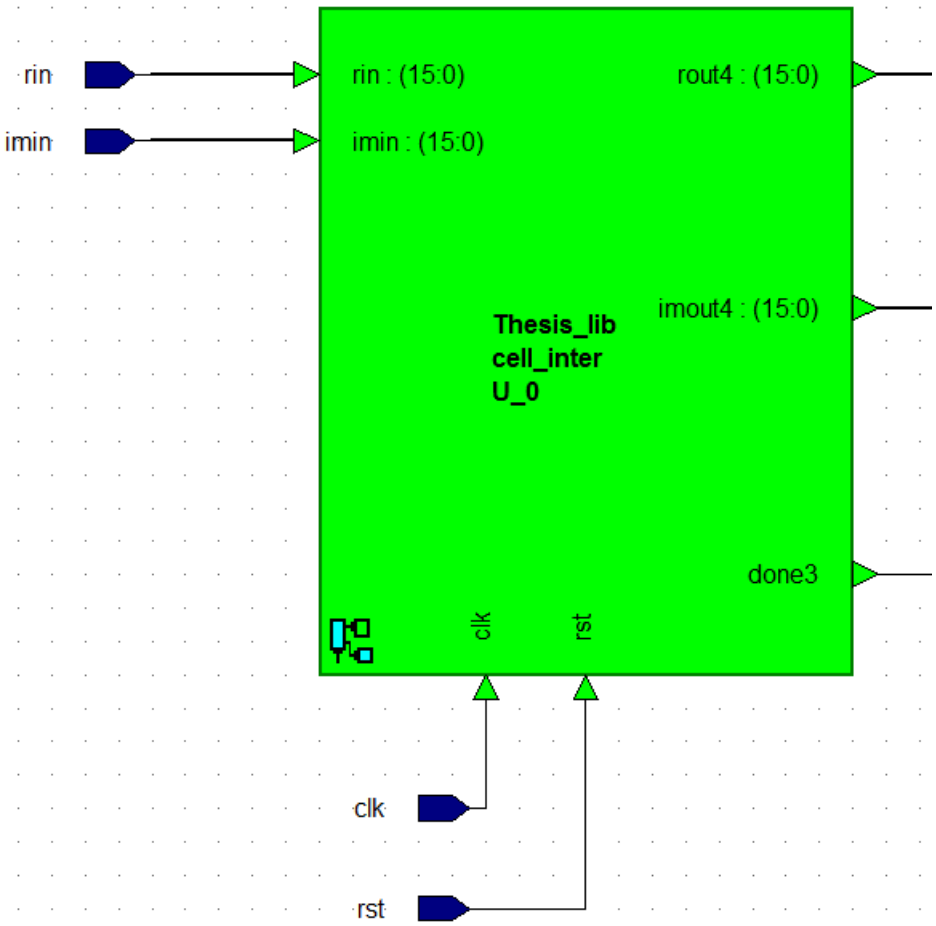

Fig. 5.5: QCT Module

5.3.1.1 Cyclic Q delay

Cyclic Q-delay is the first operation of the QCT module done on the input data stream which is the constellation rotation output. The Q delay operation is to uncorrelate the real and imaginary parts I and Q components of every constellation point. The input data stream $C_{in} = (C_{in1}, C_{in2}, \ldots, C_{in\ Ncells})$ and it delays the imaginary part by one cell. The cyclic Q delay operation output is referred to as $C_o = (C_{o1}, C_{o2} \ldots, C_{oNcells})$, where Co is given by:

$$C_o = Re(C_{in\ i}) + j\ Im(C_{in\ i+1})$$

where i takes on the values 1, 2, 3 … N_{cells}. Figures from 5.6 (a) to 5.6 (c) give a full illustration for the operation taking place in cyclic Q delay.

Figure 5.6 (a) shows the input data stream to the cyclic Q delay operation for the first clock. As in the figure it is clear that the first I component is saved in the first RAM address while its Q component is saved delayed by one Q component.

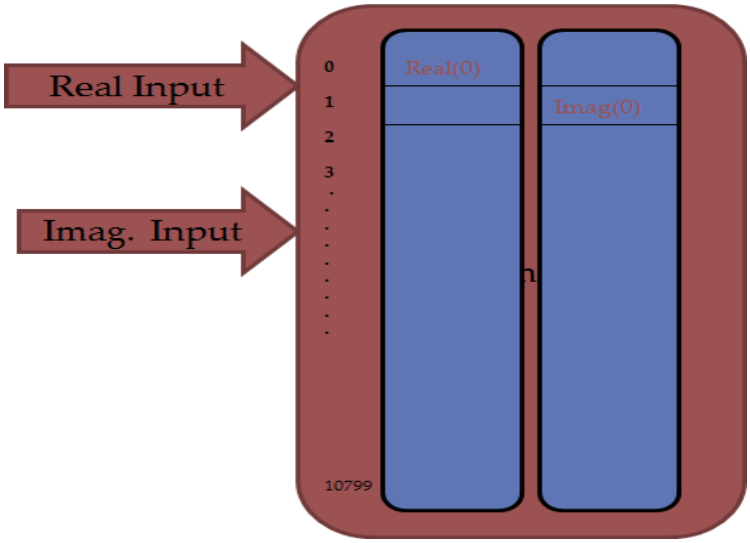

Fig.5.6 (a): Cyclic Q delay operation for the first clock

For the second clock the I component is saved in the second RAM address while its Q component is saved in delayed in the third RAM address as figure 5.6 (b) shows.

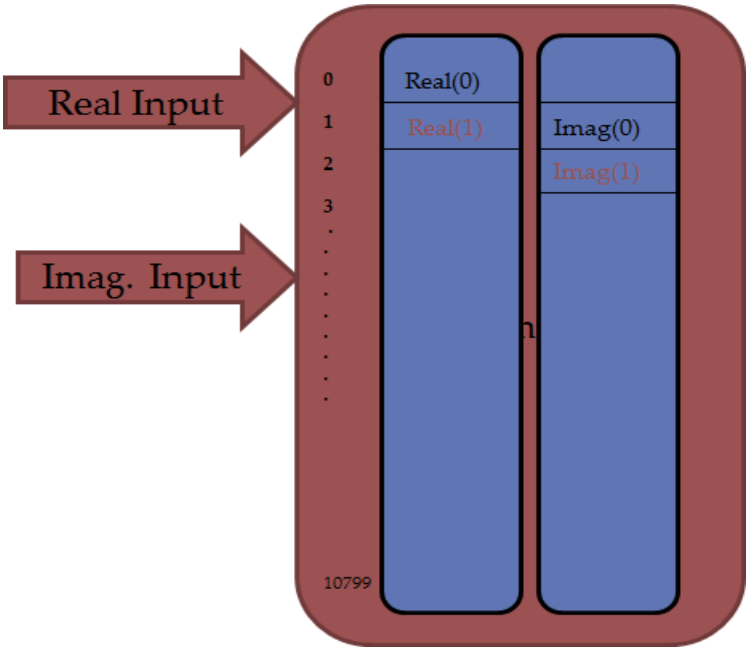

Fig.5.6 (b): Cyclic Q delay operation for the second clock

For the last input cells figure 5.6 (c) shows the completion operation for the means of the word cyclic in cyclic Q delay operation by saving the I component in address number 10799 while its Q component is cycled to be saved in the first imaginary RAM address.

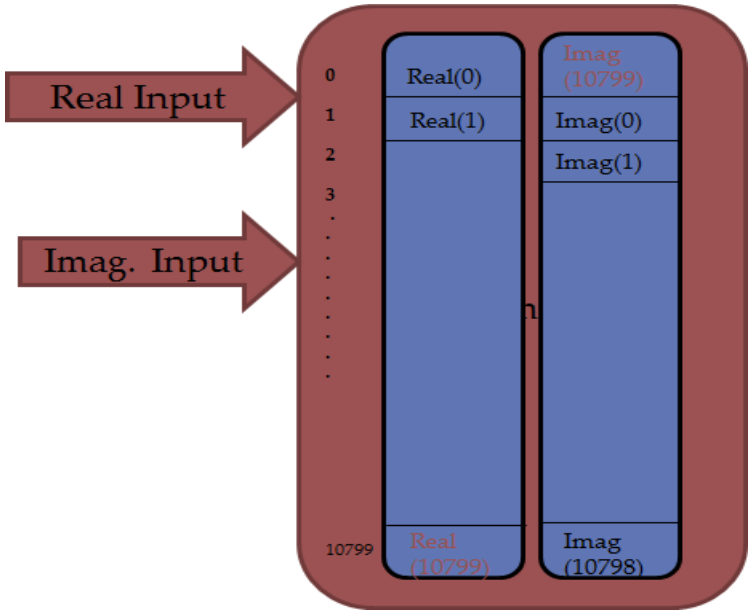

Fig.5.6 (c): Cyclic Q-delay operation for clock number 10799

To show the combination process of both the cyclic Q delay with the cell interleaver operation, the cell interleaver operation is fully explained in the following section.

5.3.1.2 Cell Interleaver

The cell interleaver operation combined with the cyclic Q delay operation both of them are applied on the input data stream on the same saving clock. The cell interleaving process is to spread the content in the time/frequency plane, such that neither impulsive noise nor frequency-selective fading affect the data stream. The cell interleaving process applies a pseudo-random permutation in order to uniformly spread the cells in the FEC code word as figures 5.7 (a) to 5.7 (c) show. The input cells to the cell interleaver take a new index which is generated from the pseudo random process.

Figure 5.7 (a) shows the cell interleaving operation for the first clock. The pseudo random permutation produces the new address the data entering on the same clock to be saved in.

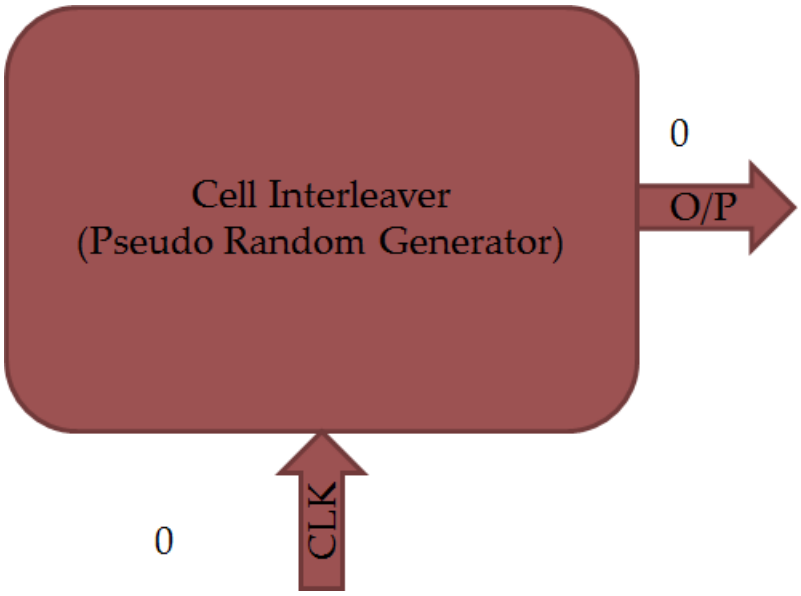

Fig 5.7 (a): Cell interleaving process for the first clock

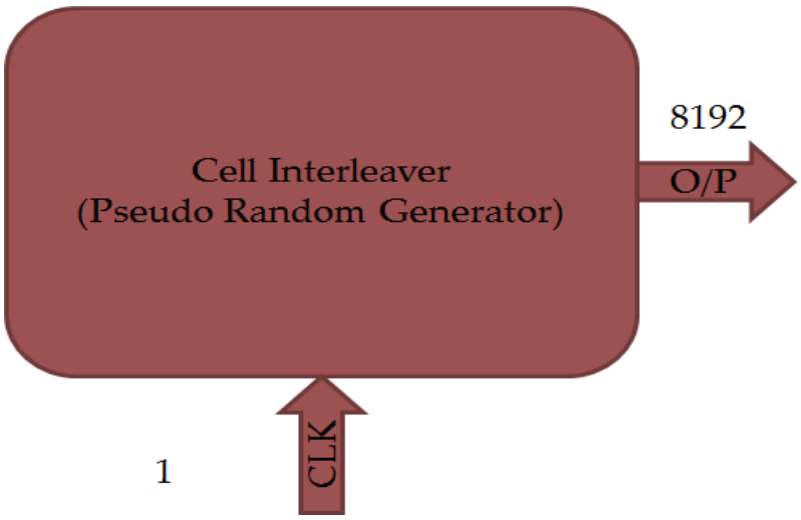

Fig 5.7 (b): Cell interleaving process for the second clock

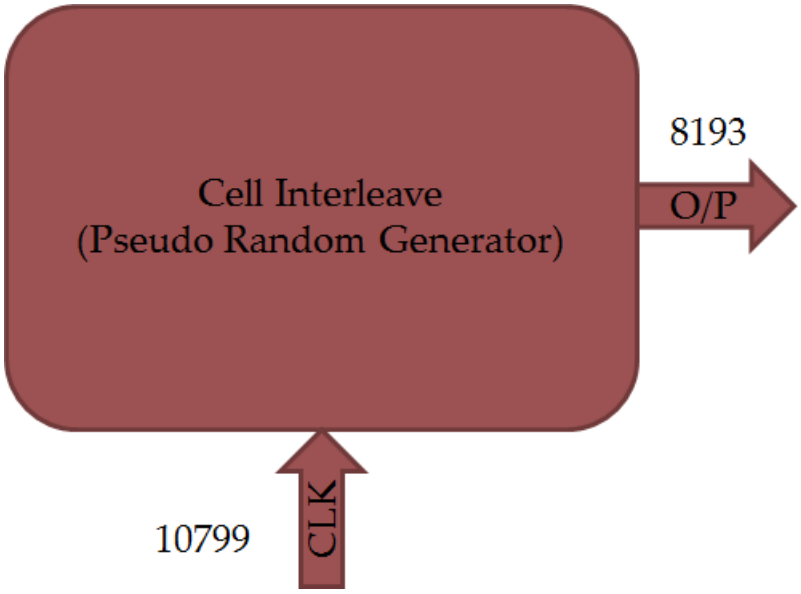

Fig 5.7 (c): Cell interleaving process for the clock 10799

5.3.1.3 Combining cyclic Q delay with cell interleaver operations

Combining the cyclic Q delay operation with the cell interleaving operation as figures 5.8 (a) to 5.8 (b) show. The first I input component as figure 5.8 (a) shows is saved in the cell interleaver permutation operation output address while its Q components are saved in the next new permutation output address and hence it is saved in front of the following I component of the next clock.

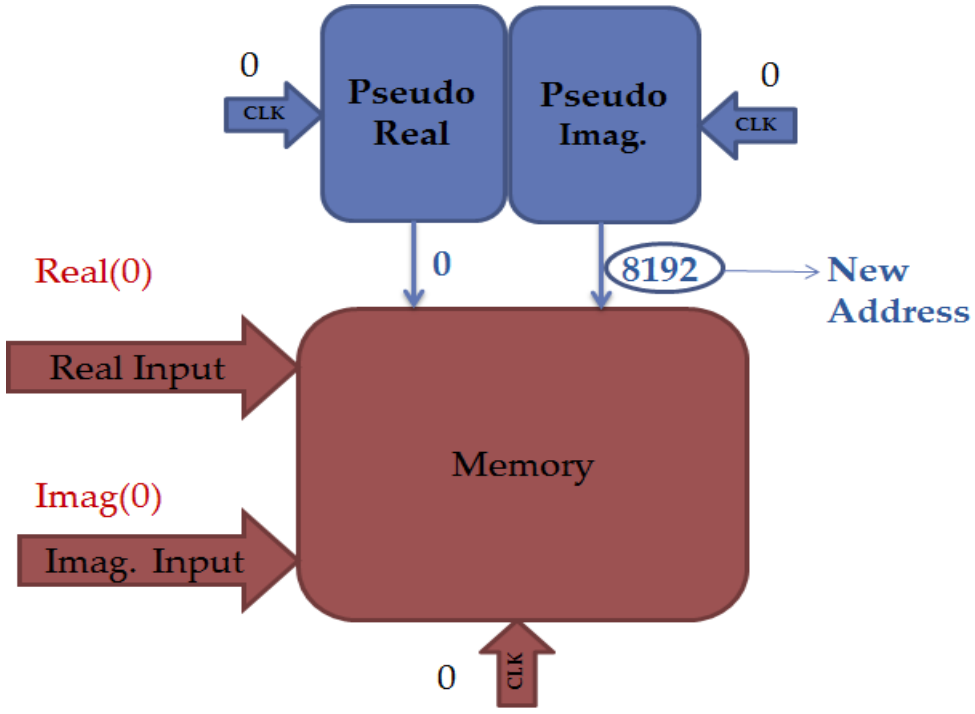

Fig. 5.8 (a): The combined operation for the first clock

For the second clock the input I component is saved in address number 8192 while its Q component is saved in address number 4096 which is in front of the following I component of clock number 3.

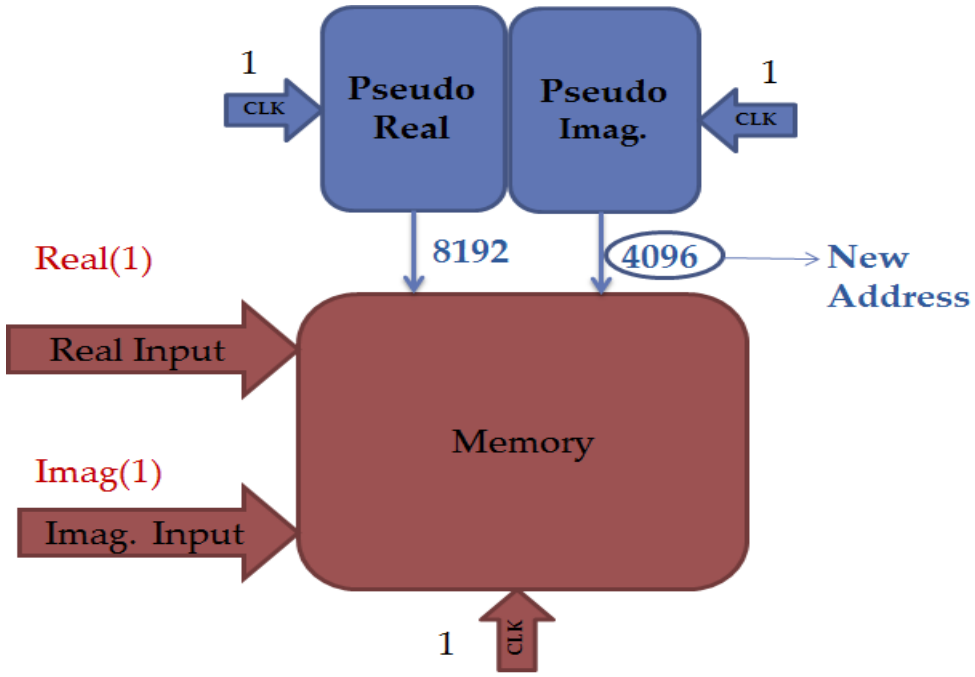

Fig. 5.8 (b): The combined operation for the second clock

For clock number 10799 which is the last clock for receiving inputs the I component is saved in address 8193 which is the last cell interleaver output address while its Q component is saved on address number 0 to complete the cyclic operation of the Q delay as figure 5.8 (c) shows.

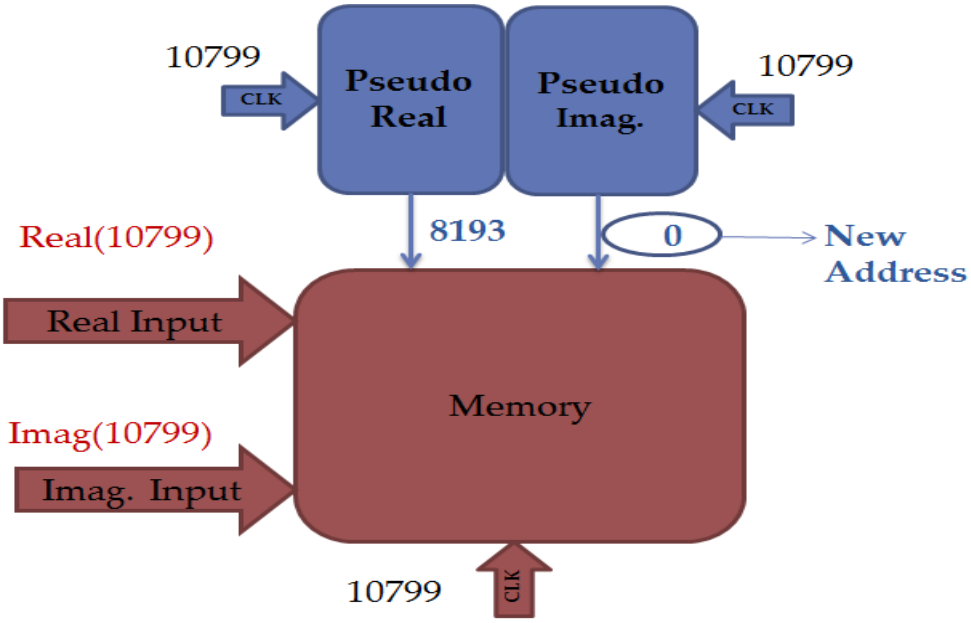

Fig. 5.8 (c): The combined operation for clock number 10799

5.3.1.4 Time interleaver

The Time interleaver is a row-column block interleaver. The time interleaving process is applied to the output data stream. The time interleaver starts its operation after the first 10799 saving clocks. The time interleaver instead of filling the input stream column wise with row wise output as in the ordinary DVB-T2 system, it reduces the delay by starting its output from address 0 as figure 5.9 (a) shows then adding 2160 to the previous address number for five times as figure 5.9 (b) shows. So it works as it is a 2160 * 5 RAM, while it works on the already saved data cells and hence reducing the delay and the hardware of the time interleaver module of the current DVB-T2 system.

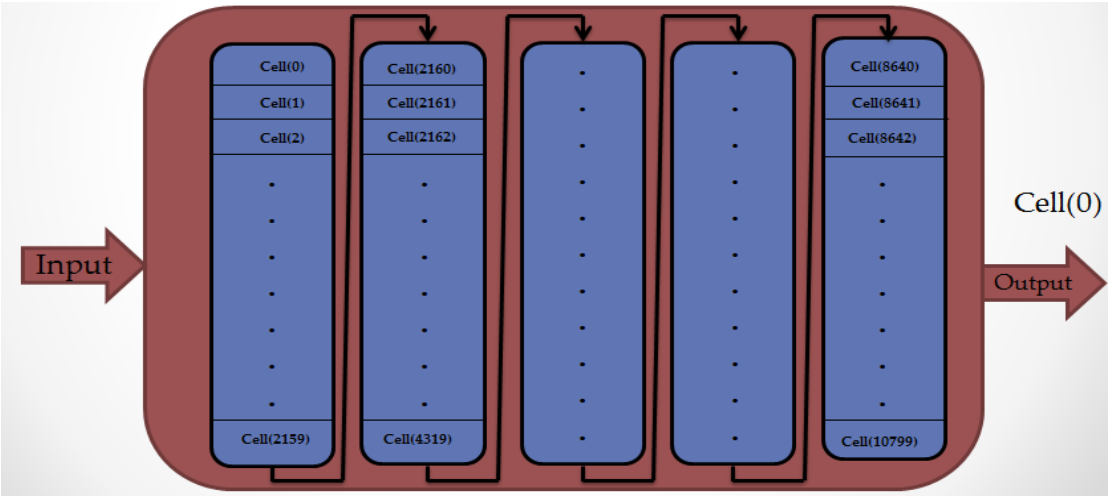

Fig. 5.9 (a): The time interleaving operation for the first clock

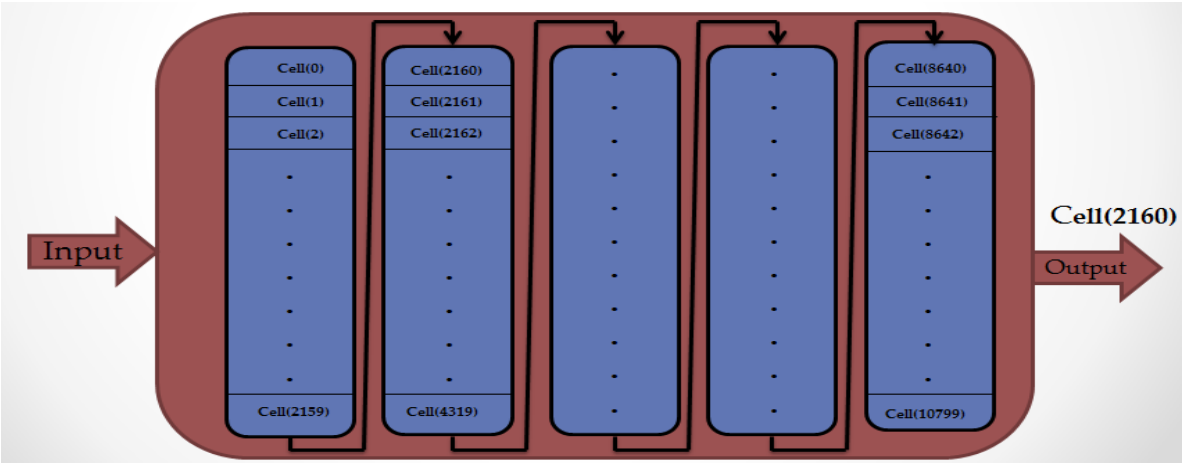

Fig. 5.9 (b): The time interleaving operation for the second clock

5.3.1.5 Combining cyclic Q-delay, cell interleaver and time interleaver (QCT module)

The time interleaving operation is added to the combination of cyclic Q delay and cell interleaving operations to form the QCT module. The QCT module applies both the cyclic Q delay with cell interleaving operations on the input data stream as explained, while the output sequence depends on the time interleaving operation. Figures 5.10 (a) to 5.10 (c) show the QCT module output for the first three clocks after the 10799 saving clocks.

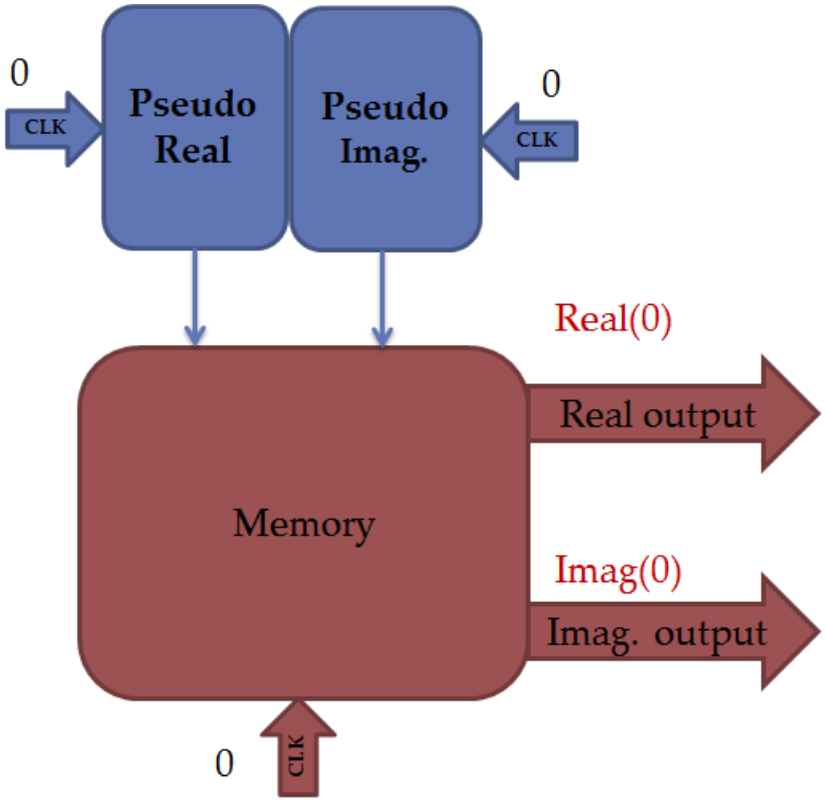

Fig. 5.10 (a): The first QCT module output after 10799 saving clocks

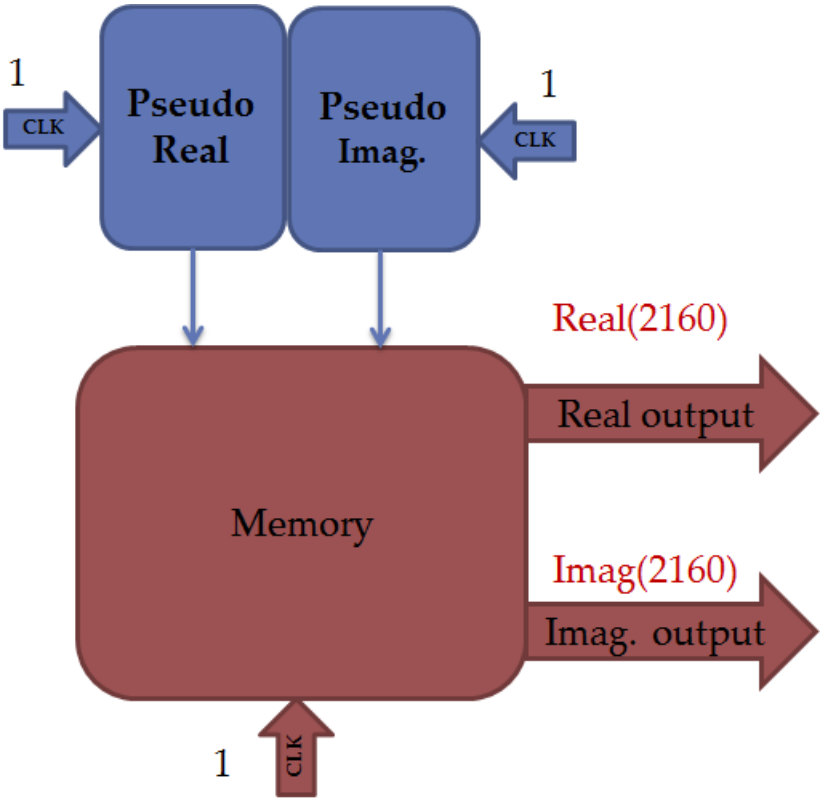

Fig. 5.10 (b): The second QCT module output after 10799 saving clocks

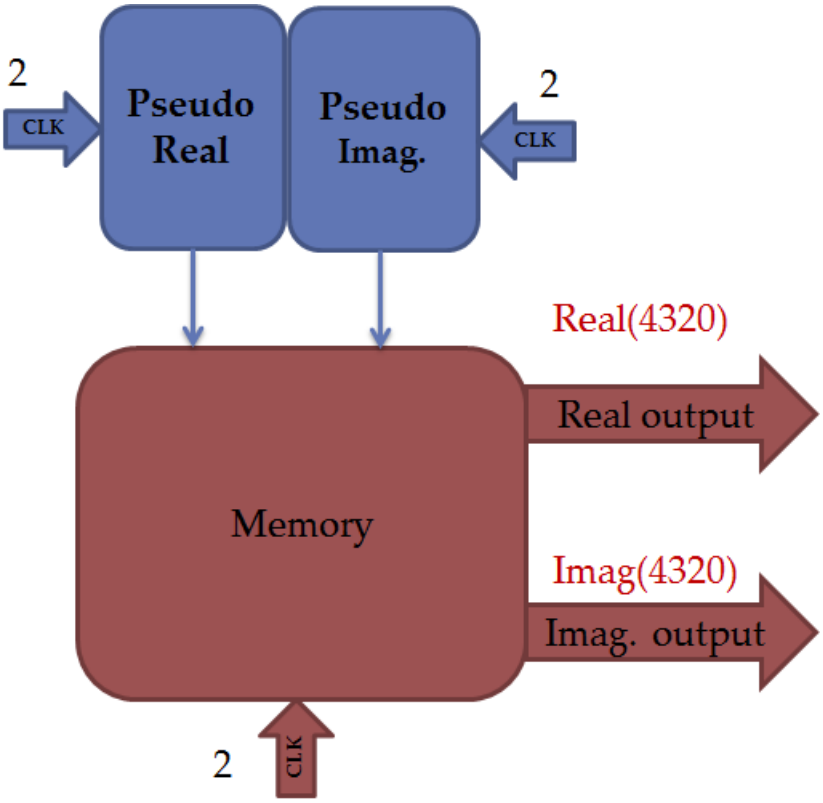

Fig. 5.10 (c): The third QCT module output after 10799 saving clocks

5.3.1.6 Implementation of the QCT module

The QCT module internally is as figure 5.11 shows. It consists of four input ports; the constellation rotation output (as an input to the cyclic q delay process) where it is divided into two ports (I and Q components), the reset port and the system clock.

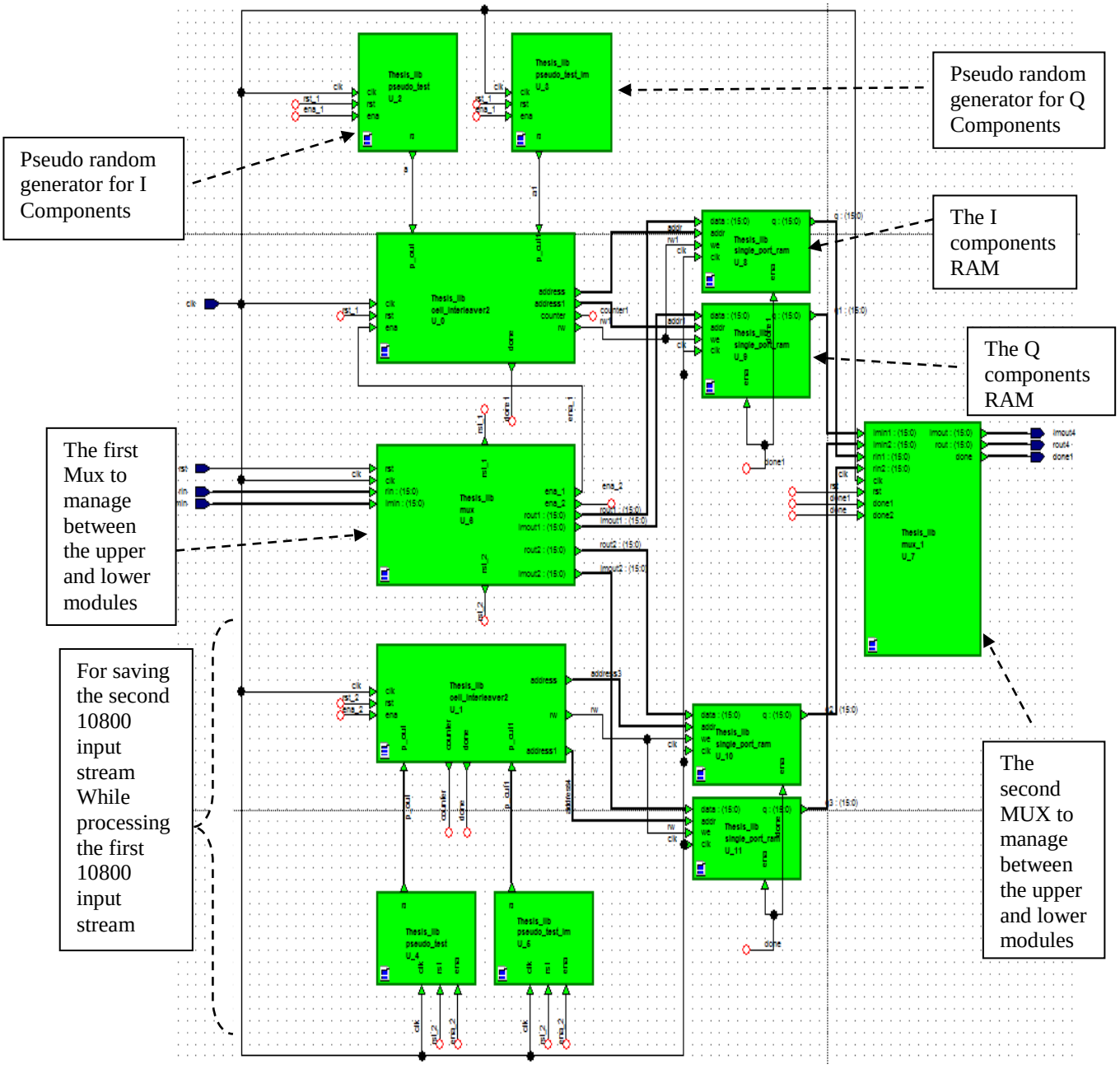

Figure 5.11: The internal QCT Module

The detailed simulation of the QCT module is in figures 5.12 (a) to 5.12 (e). The simulation is done using the ModelSim 8.1 program. The input values to the QCT module are referred to as r_{in} and im_{in}.

The input takes the first 10800 clock as shown in figure 5.8(a) and (b). The input to the module is directly saved in the module memory using both q-delay with cell interleaving process at the same time.

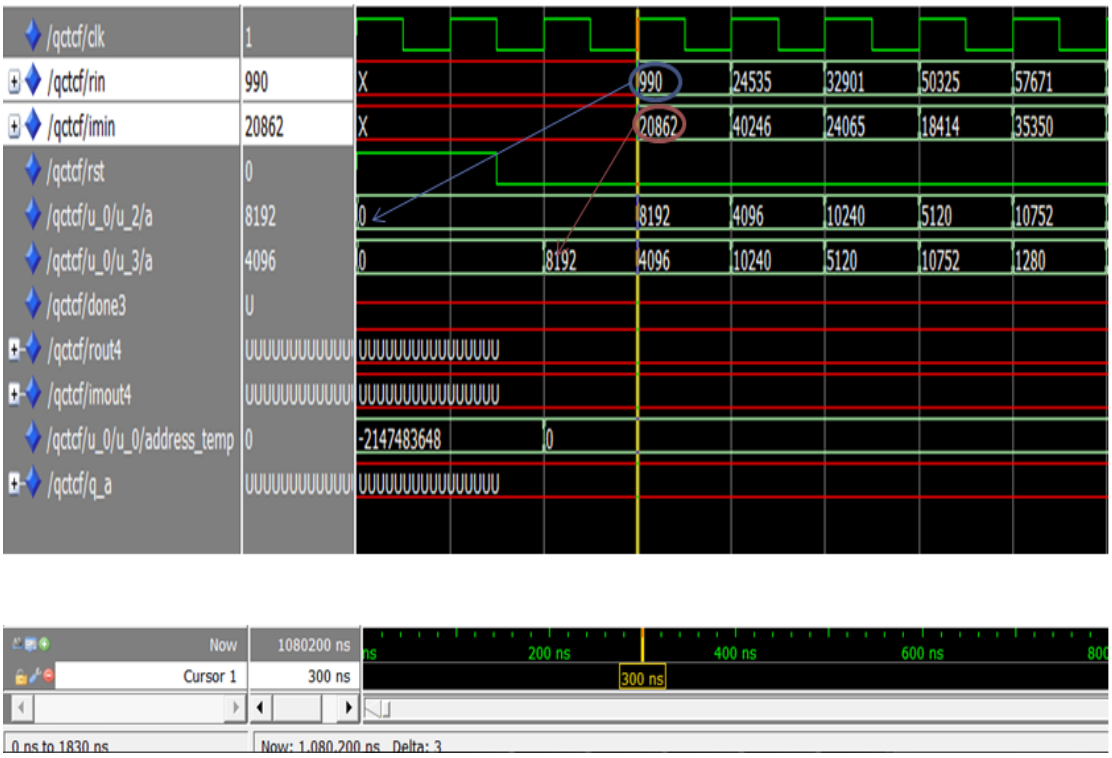

Figure 5.12 (a): The first 5 inputs to the QCT module

As the arrows on figure 5.12 (a) show the new addresses of the inputs r_{in} and im_{in} to be saved in. Figure 5.12 (b) shows that the operation of saving using both cyclic Q delay and cell interleaving operations is done as required in the right addresses. As figure 5.12 (b) the first real input is saved in address 0 while its imaginary is saved in address number 8192 using both operations of cyclic q-delay and cell interleaving.

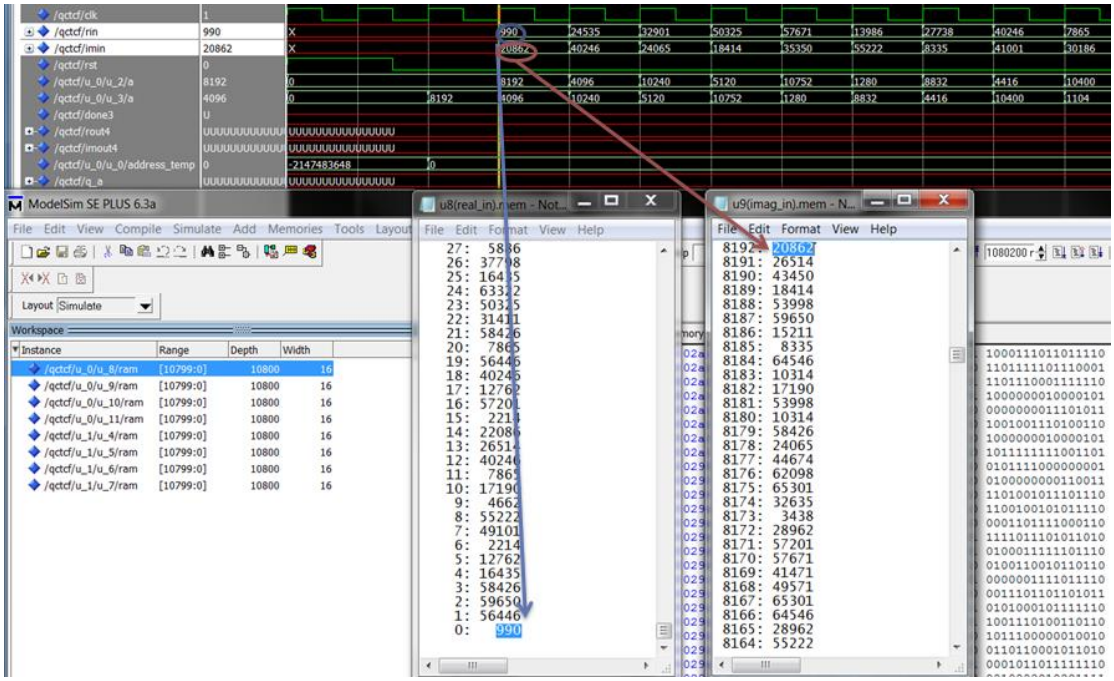

Figure 5.12 (b): The saving operation of cyclic Q delay with cell interleaving operations of the first input I and Q components

Figure 5.12 (c) shows the last five input data stream to the QCT module. The arrows on the figure show the new addresses for the last r_{in} and im_{in} to be saved in. Figure 5.12 (d) proofs that both of them are saved in right addresses.

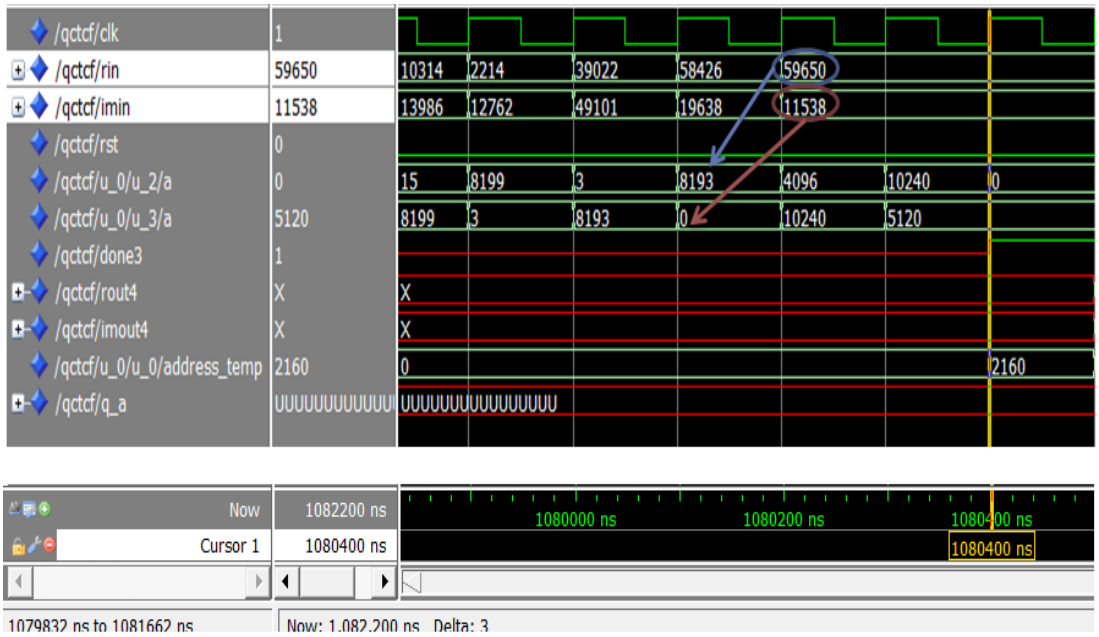

Figure 5.12 (c): The last 5 inputs to the QCT module

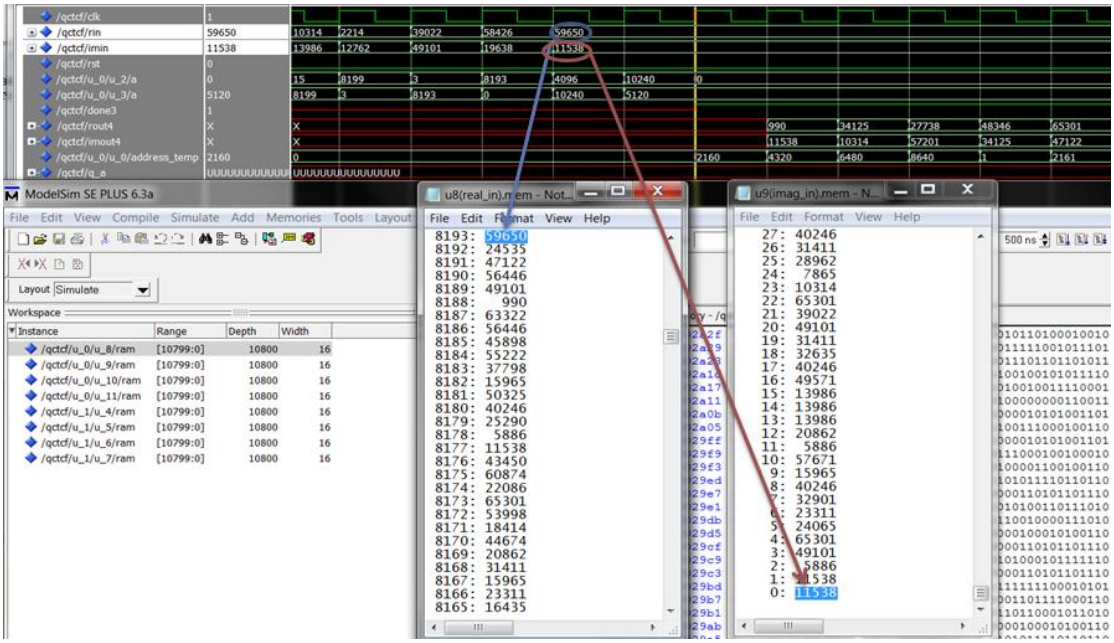

Figure 5.12 (d): The saving operation of cyclic Q delay with cell interleaving operations of the last input I and Q components

The module starts its output after 1080500 ns from its input as figure 5.12(e) shows. The time interleaving operation starts its job on the QCT module RAM. The outputs are 0, 2160 with adding 2160 to each pervious address for five counts then add one to the first address of each five pervious counts and so on for 2160 times as figure 5.12 (f) shows.

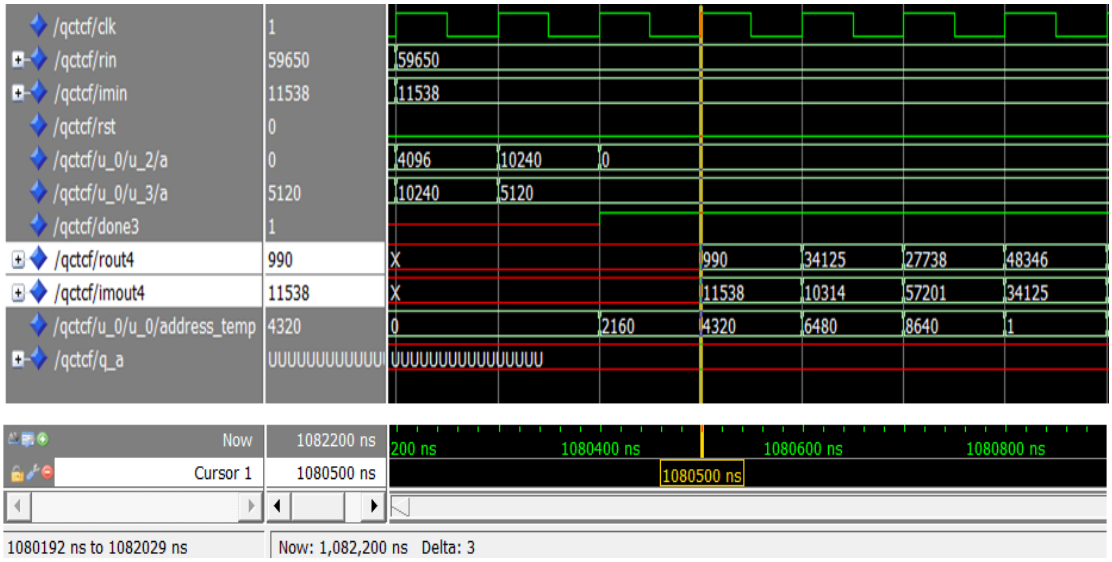

Figure 5.12 (e): The time of QCT module produce its first input

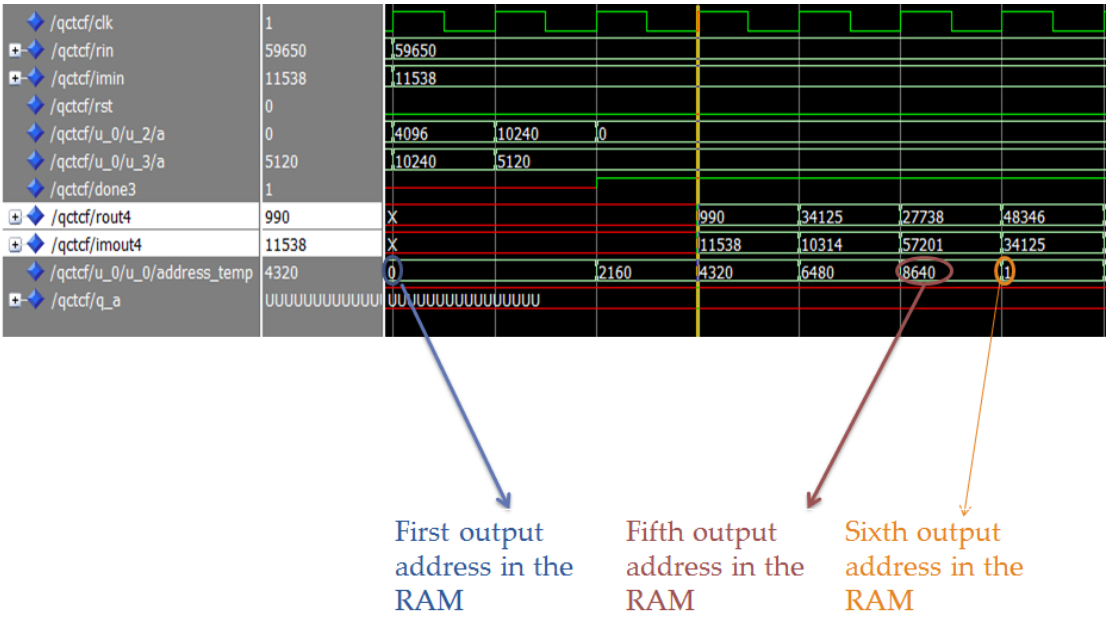

Figure 5.12 (f): The QCT module output sequence

Figure 5.12 (g) shows the first memory output using time interleaving operation.

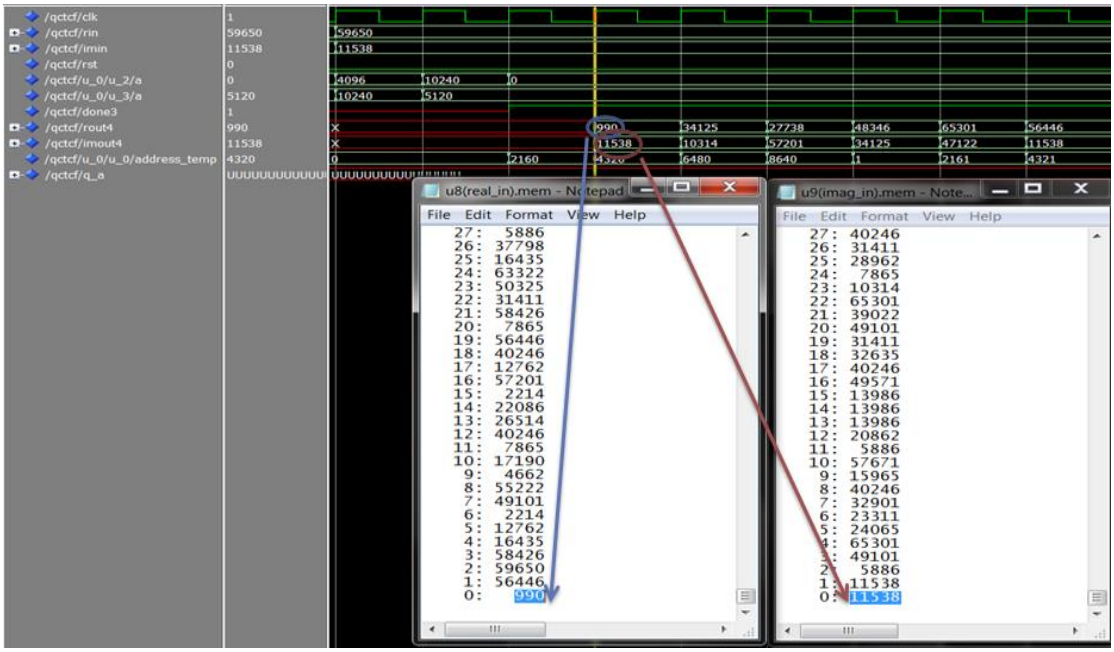

Figure 5.12 (g): The time of QCT module produce its first input

Comparing the VHDL output with the Matlab output they are the same which shows that the QCT module has made its operation as required having the advantage

of the delay and hardware reduction. The data stream output is then derived into the CF module.

Table 5.1: QCT Matlab output

	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5
r_{in}	990	34125	27738	48346	65301
im_{in}	11538	10314	57201	34125	47122

Comparing VHDL simulation output with the Matlab output we find that both outputs are the same concluding that QCT module operation is done as required.

5.3.2 The CF Module

The CF module stands for combining cell mapper with frequency interleaver. The CF module as in figure 5.13 has seven input ports with one system output (q_a) port. The system is built assuming two input PLPs. The two input PLPs have four ports for the I and Q components. The CF module makes the operation of both cell mapper and frequency interleaver at the same time cutting down the overall system delay.

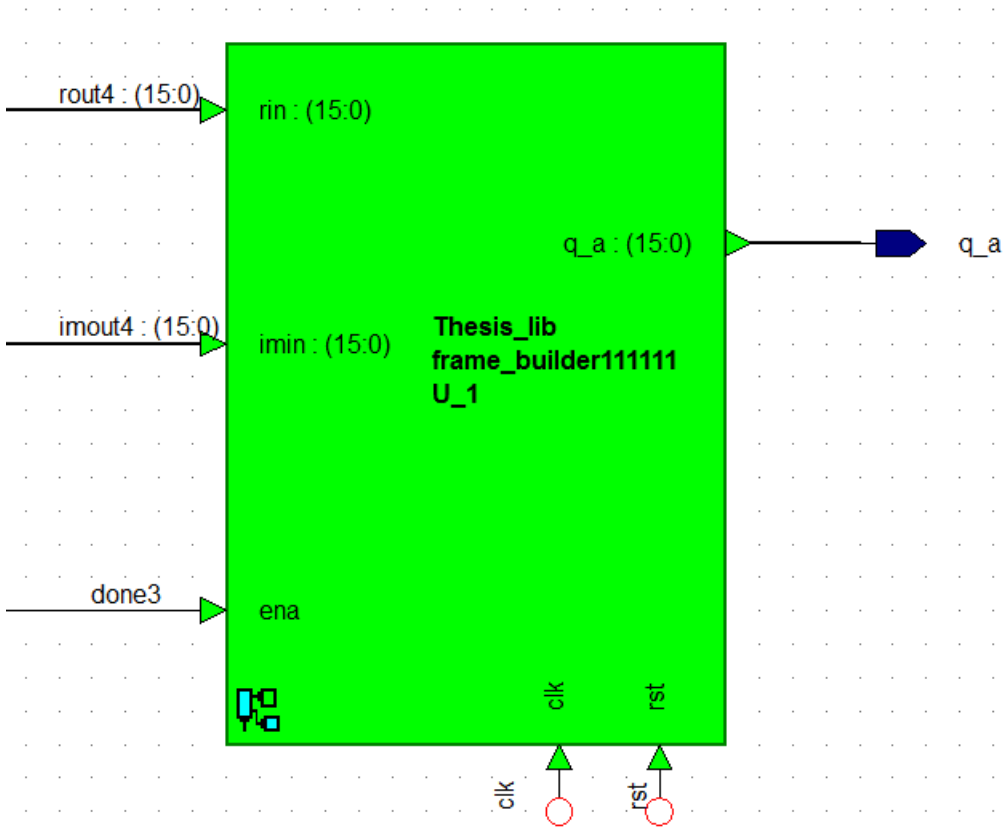

Figure 5.13: The CF module

5.3.2.1 The cell mapper

The cell mapper maps the input stream into T2 frames. The T2 frames are grouped together into T2 super frame. The cell mapper has two input PLPs each has its I and Q components. The cell mapper in the proposed CF module makes the operation faster than in the current DVB-T2 system. The cell mapper saves the input from both PLPs on the same RAM unlike the current DVB-T2 cell mapper which saves all of them before combining both of them. Figures 5.14 (a) and 5.14 (b) show the cell mapper of the proposed module operation for the first clock and clock number 5400.

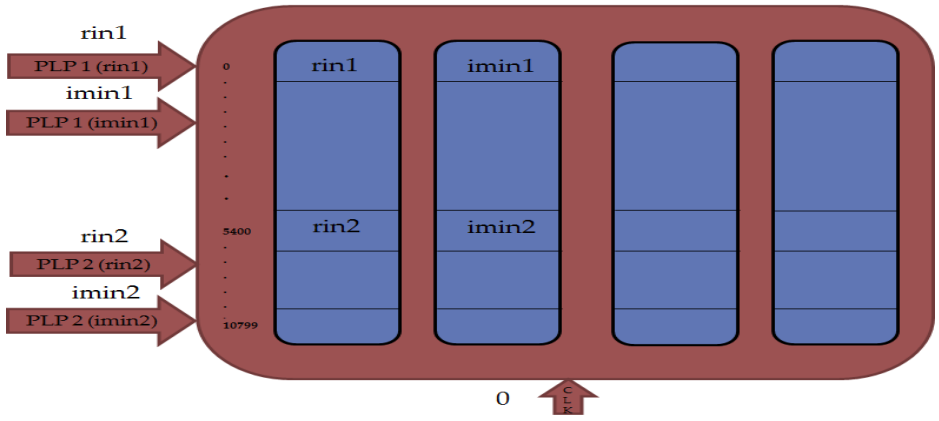

Figure 5.14 (a): The cell mapper operation of the first clock

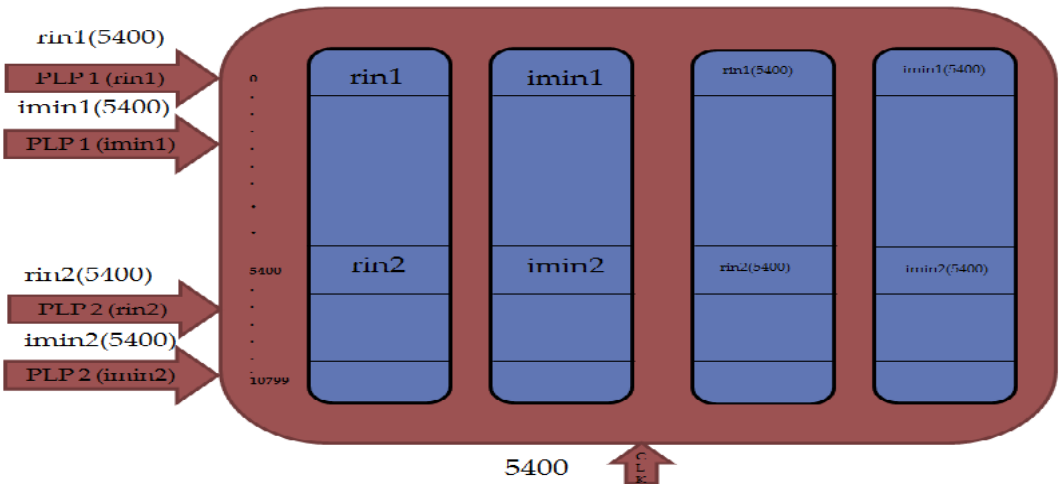

Figure 5.14 (b): The cell mapper operation of clock number 5400

5.3.2.2 The frequency interleaver

The frequency interleaver makes an interleaving process similar to that in the cell interleaver module. It divides the input data stream from multiple PLPs saved by the cell mapper into even and odd steams. The frequency interleaver then applies the same permutation function used in the cell interlaver module on both streams. The output is then grouped together for the OFDM generation operation. Figures 5.15 (a) and 5.15 (b) show the frequency interleaver operation of the CF module.

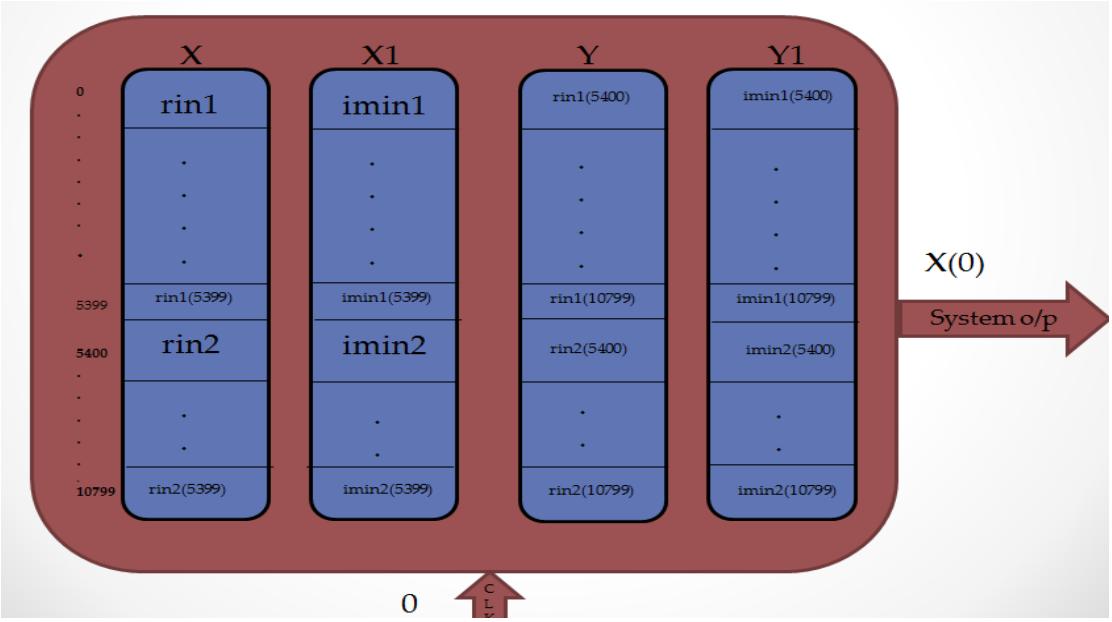

Figure 5.15 (a): The frequency interleaving operation of the first output

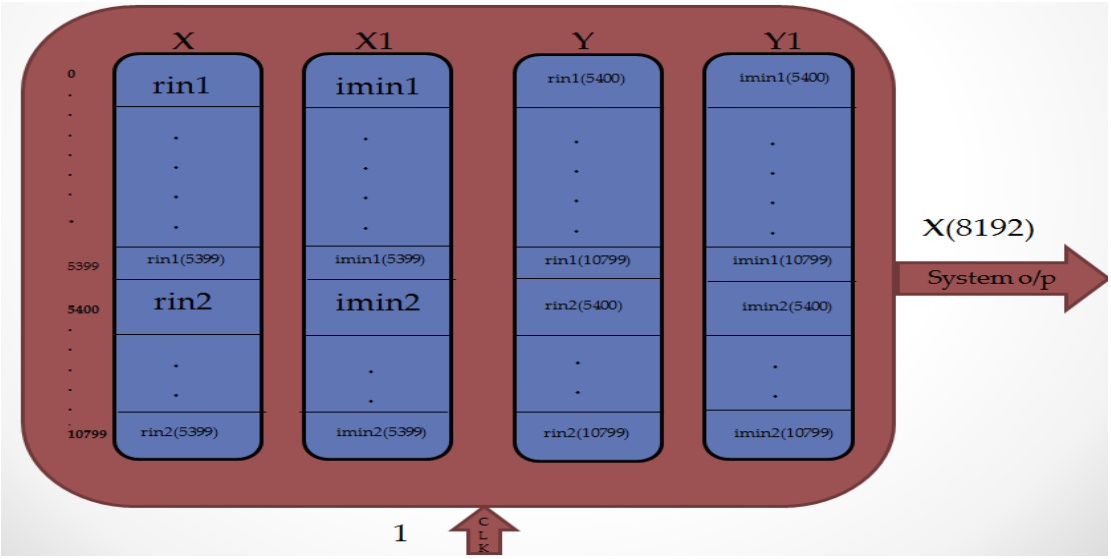

Figure 5.15 (b): The frequency interleaving operation of the second output

5.3.2.3 Combining the cell mapper with the frequency interleaver

Combining the cell mapper with the frequency interleaver to reduce the overall system delay, in addition to the large hardware reduction. Figure 5.16 shows the combination of the two operations to be held by one module.

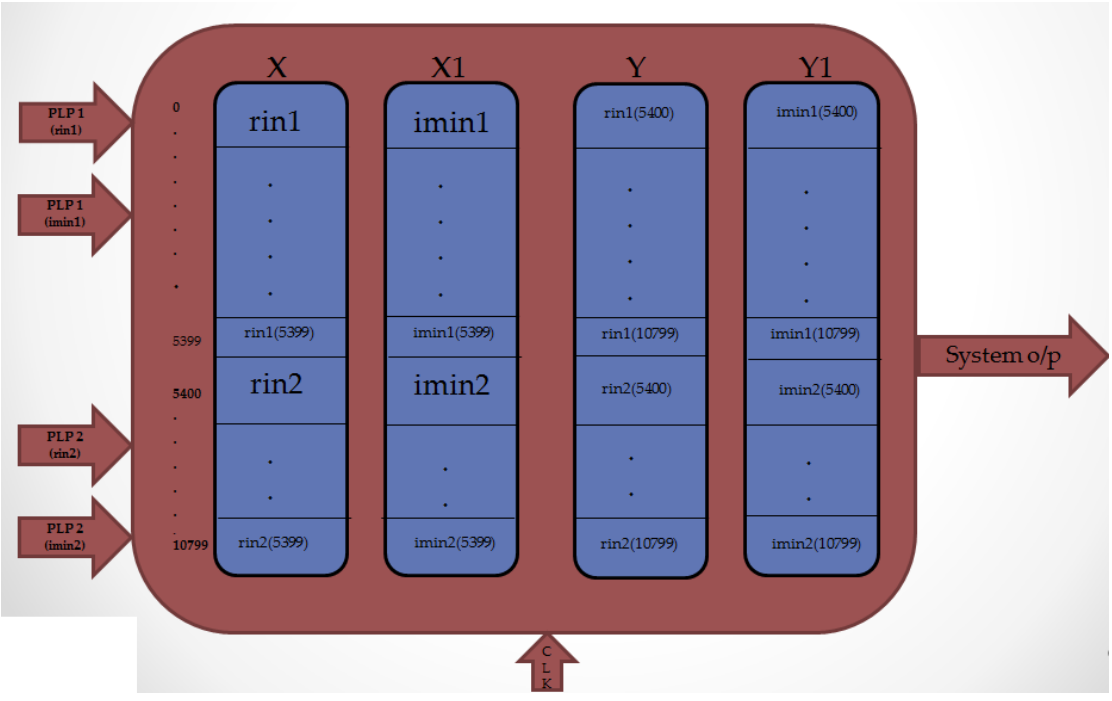

Figure 5.16: The combination of cell mapper with frequency interleaver operations

5.3.2.4 Implementation of the CF module

The implementation of the cell mapper and frequency interleaver integration is figure 5.17. It has five input ports with one system output port.

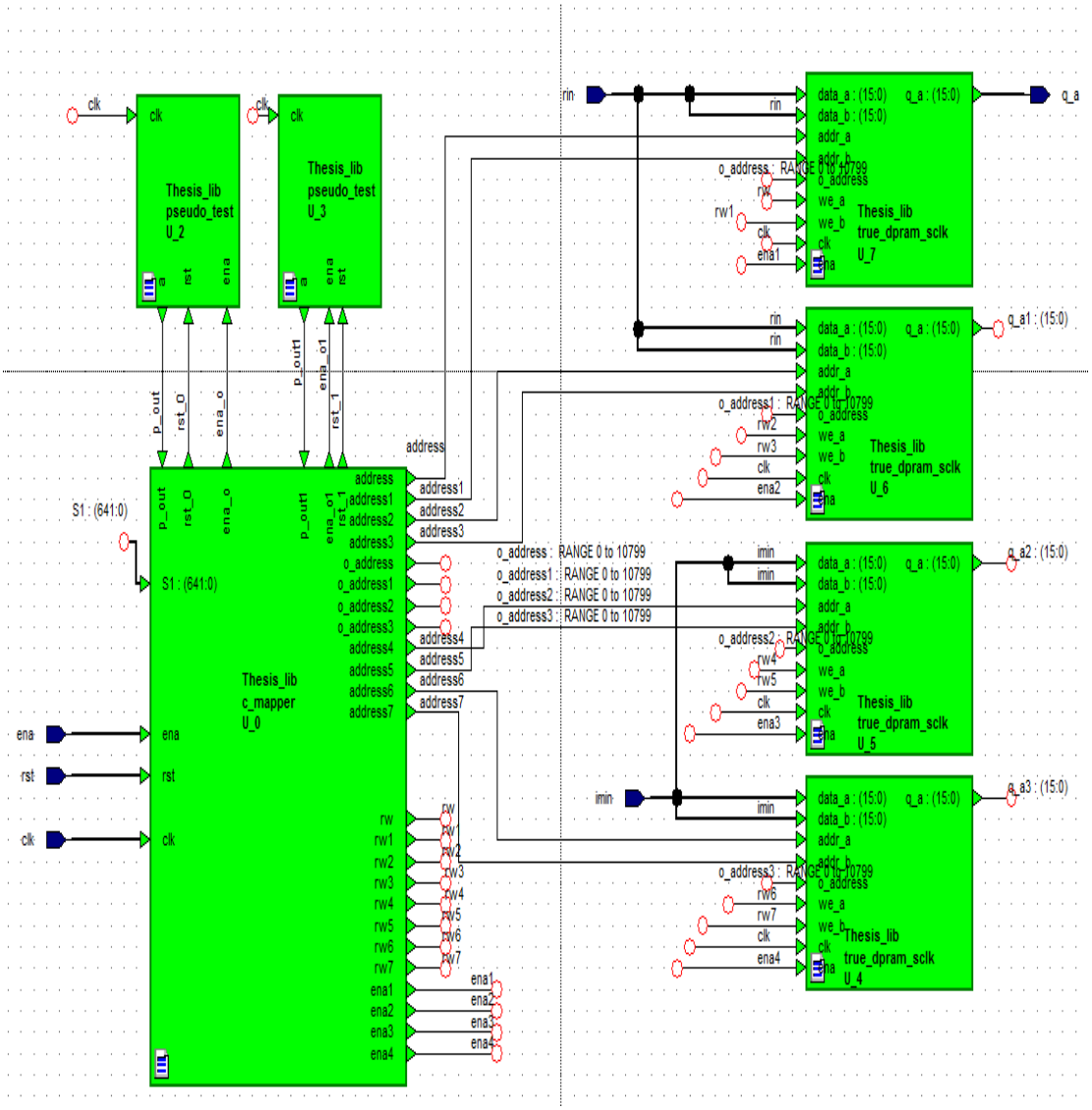

Fig. 5.17: The CF module internally

The cell mapper and frequency interleaver integration module starts to take its input after 10800 clocks from the start of the system input. It takes the QCT output data stream as an input. The QCT module takes 10800 clocks in the beginning of the system input stream for saving, delaying and interleaving then starts its output. The cell mapper and frequency interleaver integration module is then employed after QCT operation starts its output. It makes both operations of cell mapping and frequency

interleaving in 10800 clocks before it starts its output which is our system output. After 2160500 clocks from the system start up the system output begins. Figures 5.18 (a) and 5.18 (b) show the first two system outputs.

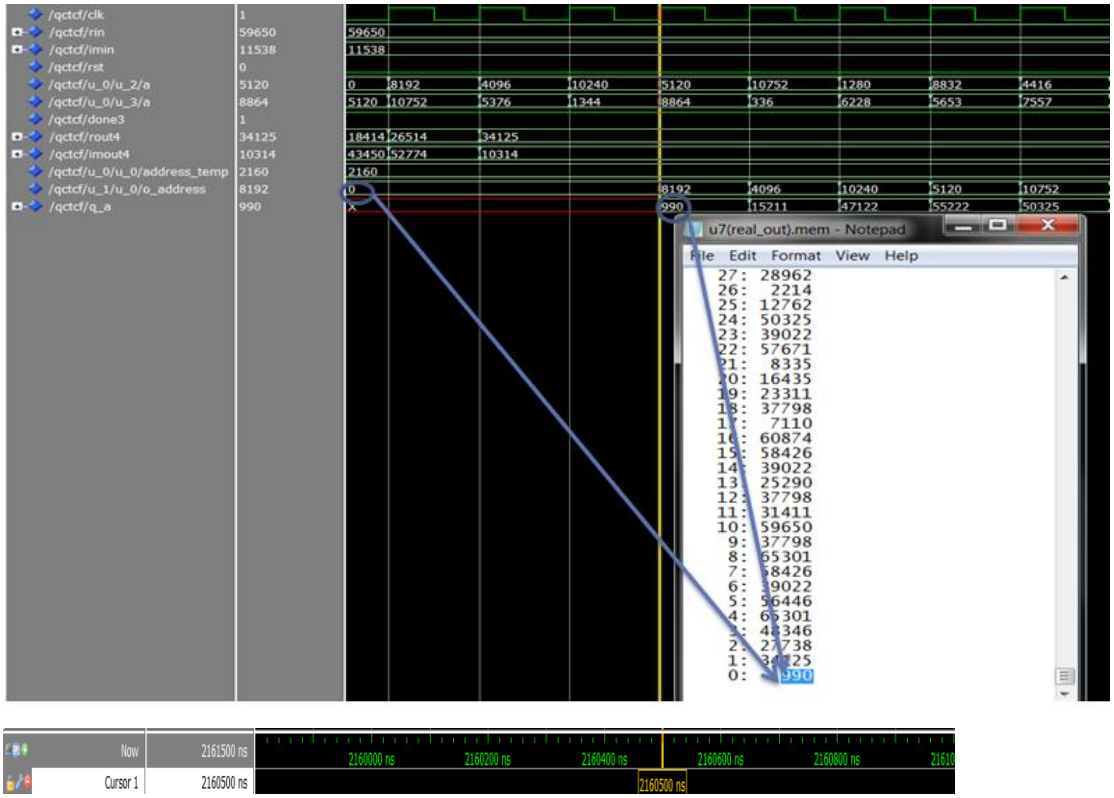

Fig. 5.18 (a): The QCTCF module first output

The system output begins by the data of addresses 0, 8192, 4096 of the first column of the RAM as shown in figures 5.18 (a) and 5.18 (b).

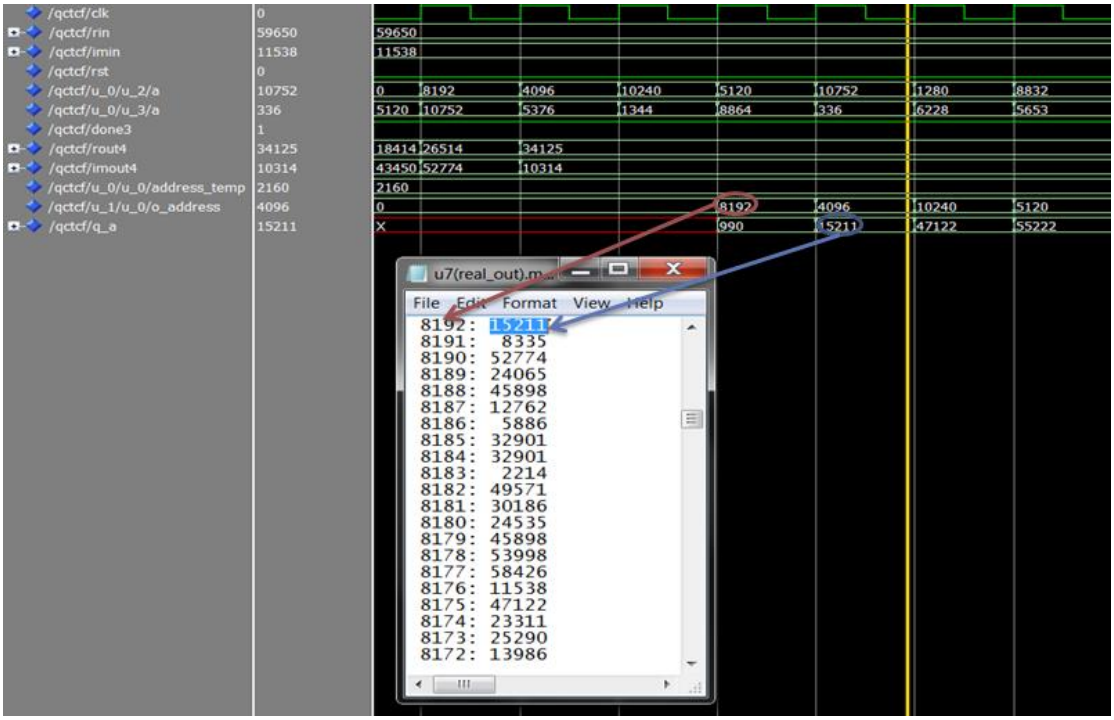

Fig. 5.18 (b): The QCTCF module second output

Table 5.2: QCTCF Matlab output

	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5
r_{in}	990	34125	27738	48346	65301
im_{in}	11538	10314	57201	34125	47122

Comparing VHDL simulation output with the Matlab output we find that both outputs are the same concluding that CF module operation is done as required and hence the QCTCF module.

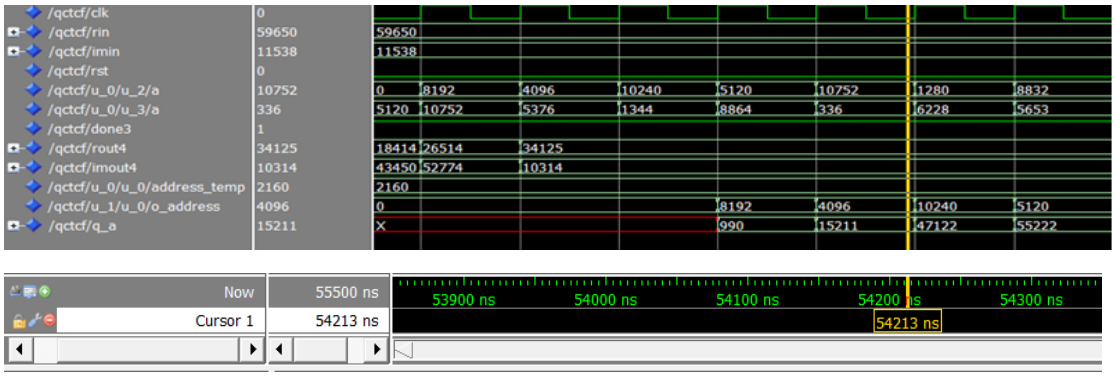

Figure 5.19: Simulation of DVB-T2 without using QCTCF module

Comparing between figure5.19 which shows the output starting at 54600ns with the system using QCTCF module, a large delay is noticed when using the ordinary system with respect to using the one with QCTCF module whose output starts at 21600ns showing the large delay cut off happens when using the QCTCF module in the DVB-T2 system.

5.4 Synthesis

In this dissertation the QCTCF module was synthesized. Synthesis was performed using QuartusII 13 to be downloaded on an FPGA. The Design has fitted on Cyclone IV GX EP4CGX22CF19C6. Results as shown in fig. 5.14 show that in the uses 4% of the total logic elements from the chip size where the number of input/output pins is 50, while the number of registers used are 365. The total memory bits used are 45%.

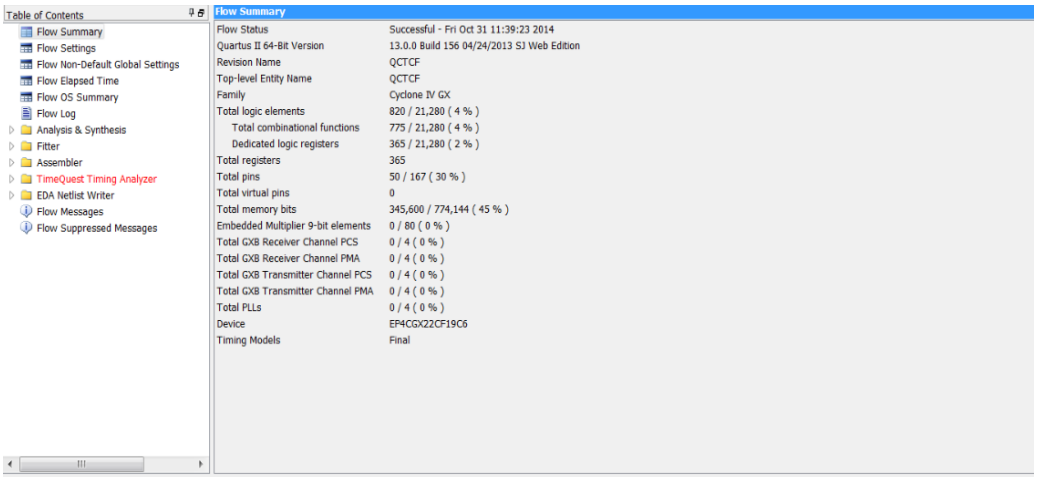

Figure 5.19: QCTCF Module synthesizing flow summary

5.5 Conclusion

As a conclusion, this chapter introduces the hardware part of this thesis. This chapter presents five integrated modules. The first module implemented is the integration of q-delay, cell interleaver and time interleaver, the second module is an integration of the cell mapper and frequency interleaver modules. A VHDL code was written for every module using the FPGA ADV.PRO 8.1, the modules were also simulated using the MODEL SIM, finally the integrated modules techniques were synthesized. Synthesis shows that the integration done on these five modules into a single module decreases both the overall system delay in addition to the DVB-T2 system hardware.

Chapter 6
Conclusions and Future Work

6.1 Conclusions

This thesis is divided into four chapters. The first chapter is considered an introduction to the Digital television standards. The 3 main television standards were mentioned with the brief description of their data processing. The DVB standard was the main focus for the rest of the chapter. The different standards of the DVB system were discussed showing the differences and similarities between them.

In chapter three, the Digital video broadcasting terristrial Second Generation was introduced. The key features of the system were fully described. The DVB-T2 system uses for forward error correction technique two concatenated encoders which are the BCH encoder and the LDPC encoder. There are a lot of modulation schemes available like 16 QAM- 64 QAM and 256 QAM. DVB-T2 uses four interleavers to ensure that the system is highly protected against burst errors. From these feature the DVB-T2 system has increased its channel capacity to 30% than that reached by the DVB-T standard. In chapter four, the simulation of the proposed DVB-T2 system is introduced .The simulation was done on the Matlab program. Every block within the system was discussed showing the input and output dimension. The values of parameters used are mentioned.

The system was discussed for 64 QAM mapping. Finally the results of the system are presented. The results focused on the cyclic Q-delay, cell interleaver, time interleaver, cell mapper and frequency interleaver. In chapter five, five modules have been integrated into one

module. A VHDL code has been written for every module using the FPGA 8.1 ADV.Pro. Every module was simulated by the Modelsim 5.3 program and verified with the results of the Matlab program. Finally synthesizes is introduced using Quarus 13.

6.2 Future Work

The future work will be the whole DVB-T2 system implementation.

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